

Model Name: GA-Z97X-SOC

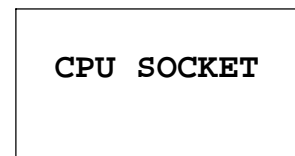
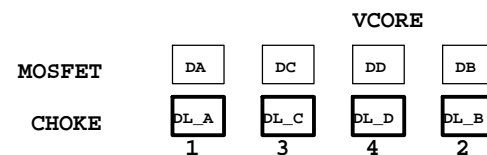
SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCH HDMI/DP
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*8 SLOT
17	PCI EXPRESS*1 SLOTS X1
18	PCI EXPRESS X8 X4 SWITCH
19	PCI EXPRESS*4 SLOT (CPU)
20	PCI EXPRESS*4 SLOT (PCH)
21	ITE 8892
22	PCI SLOT 1&2
23	ALC1150
24	REAR AUDIO JACK
25	Dual BIOS
26	IR3564A PWM
27	IR3550-VCORE

Rev 1.0

SHEET TITLE

28	IR3550-DDR POWER
29	5VDUAL, 3VDAUL, ERP
30	DISCRETE POWER
31	I/O ITE8620
32	KB/USB3,R_USB
33	F_PANEL ,COM , PHOT
34	F_USB 2.0
35	F_USB 3.0
36	ATX POWER
37	HWM, FAN CTRL
38	INTEL LAN I217
39	Highly switch
40	RST, PWR, CLR_CMOS,NCT3933
41	IT 8791
42	EC FAN CTRL
43	OC POWER
44	SATA EXPRESS
45	VGA
46	TABLE

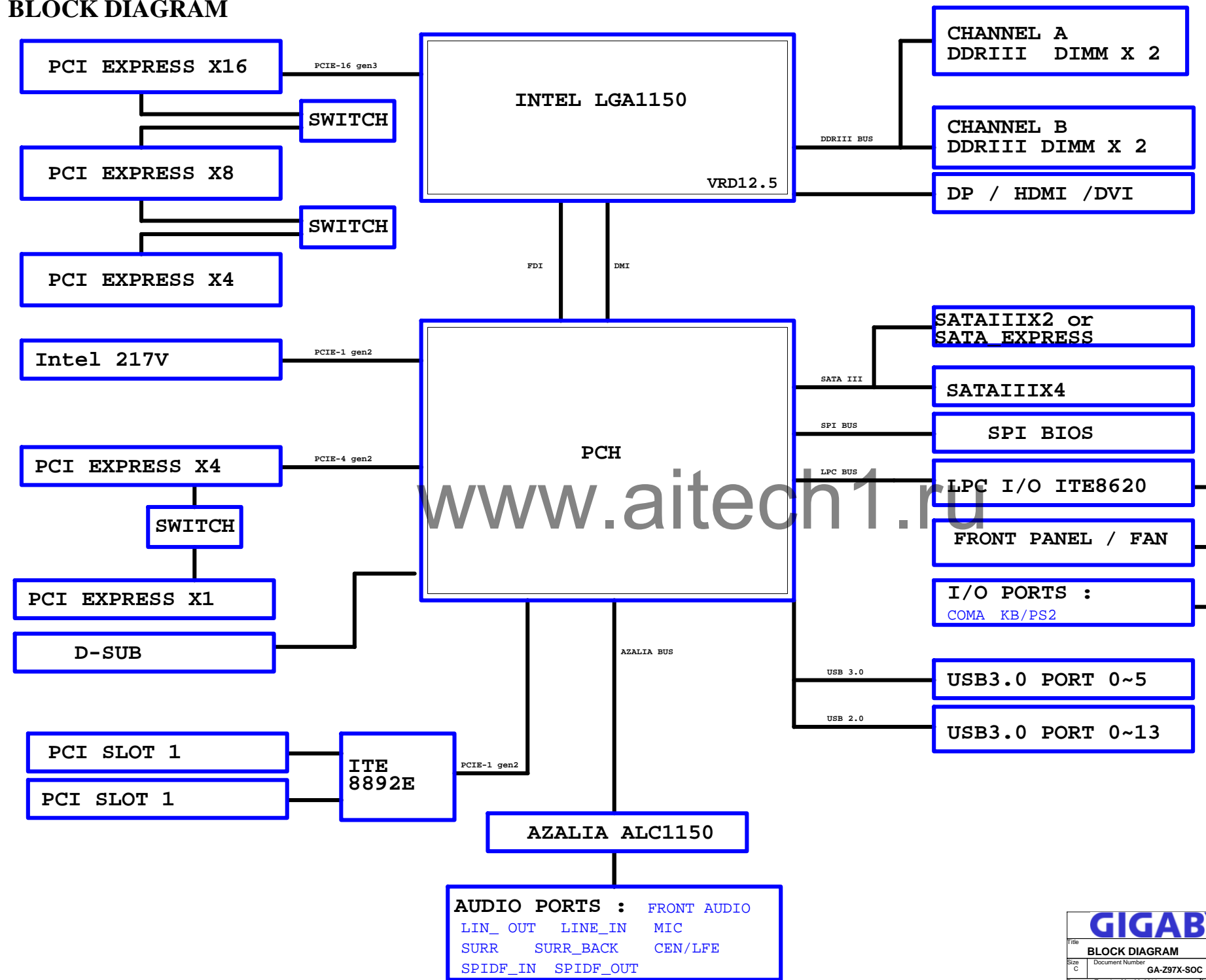


GIGABYTE™		
Title: Cover Sheet		
Size: Custom	Document Number: GA-Z97X-SOC	Rev: 1.0
Date: Tuesday, May 06, 2014	Sheet: 1	of 47

Component value change history

[illegible][illegible]

BLOCK DIAGRAM

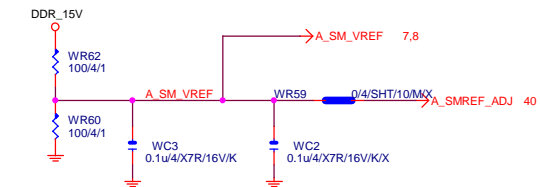


CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	NORM	Reverse	LANE REVERSAL[01,x16]
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

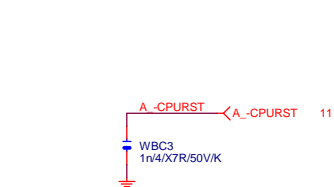
CFG6	CFG5	PCIE CONFIG
1	1	1X16, Default
1	0	2X8
0	1	RSVD
0	0	X8_X4_X4

CFG 0-17 all internal PULL-UP

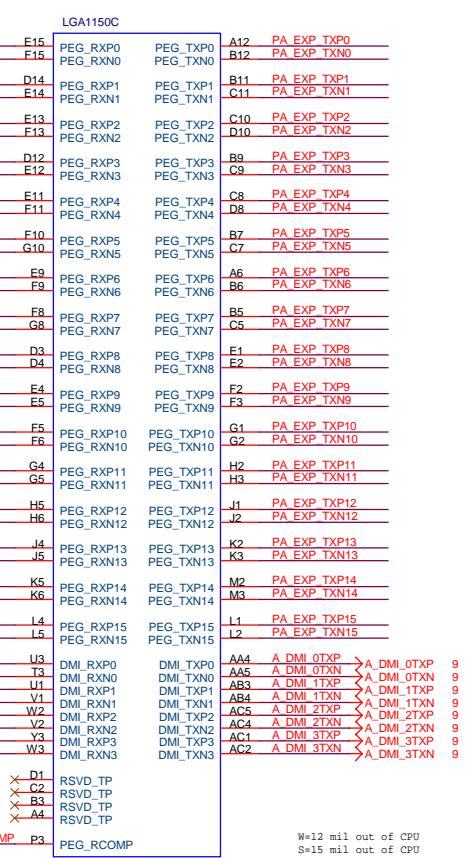
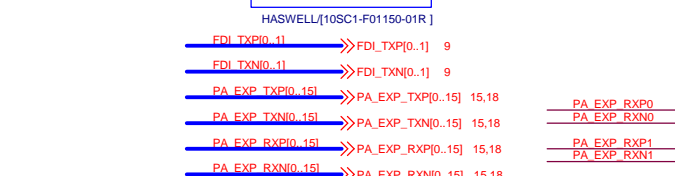
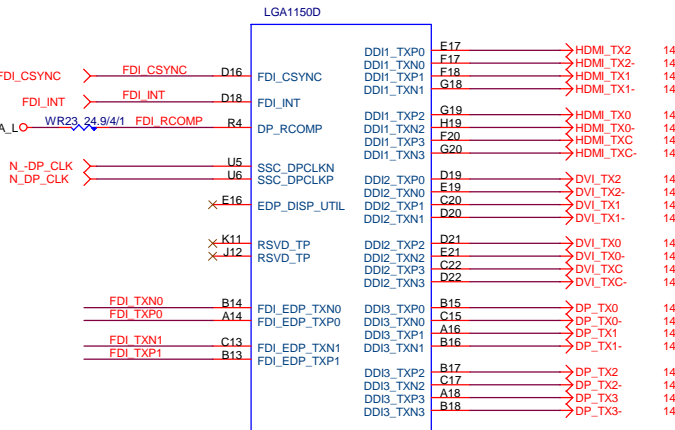
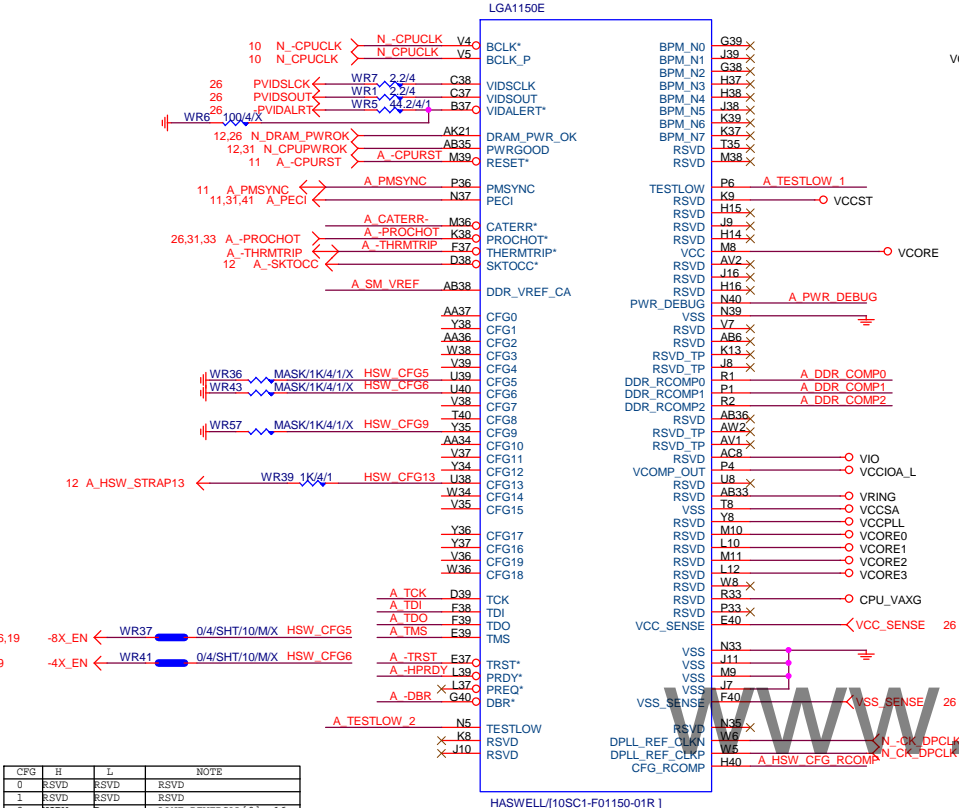
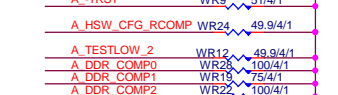
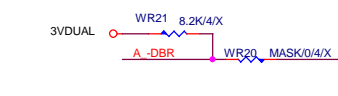
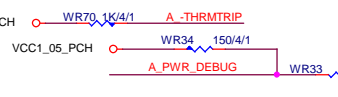
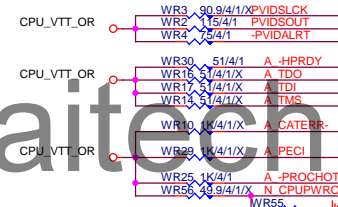
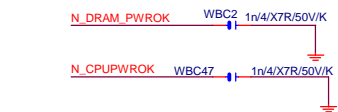
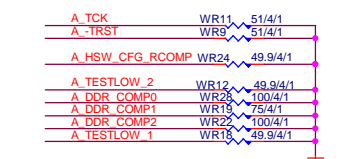
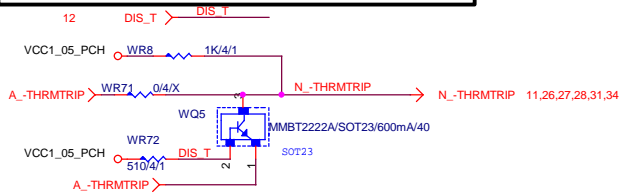
SM_REF



-CPURST



THRMTRIP DISABLE FOR Z97 OVERCLOCK



Title
CPU LGA1150-A

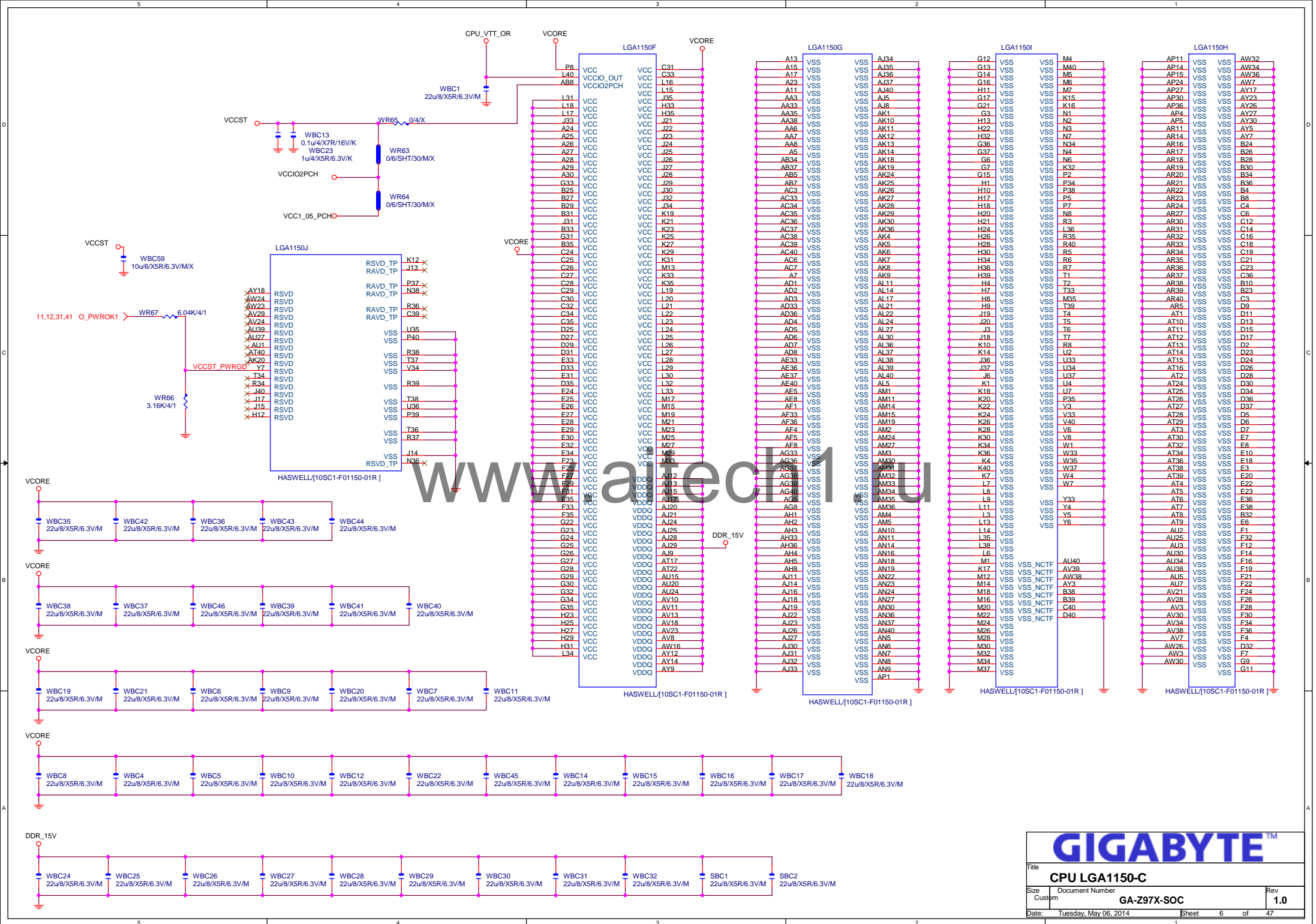
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Custom

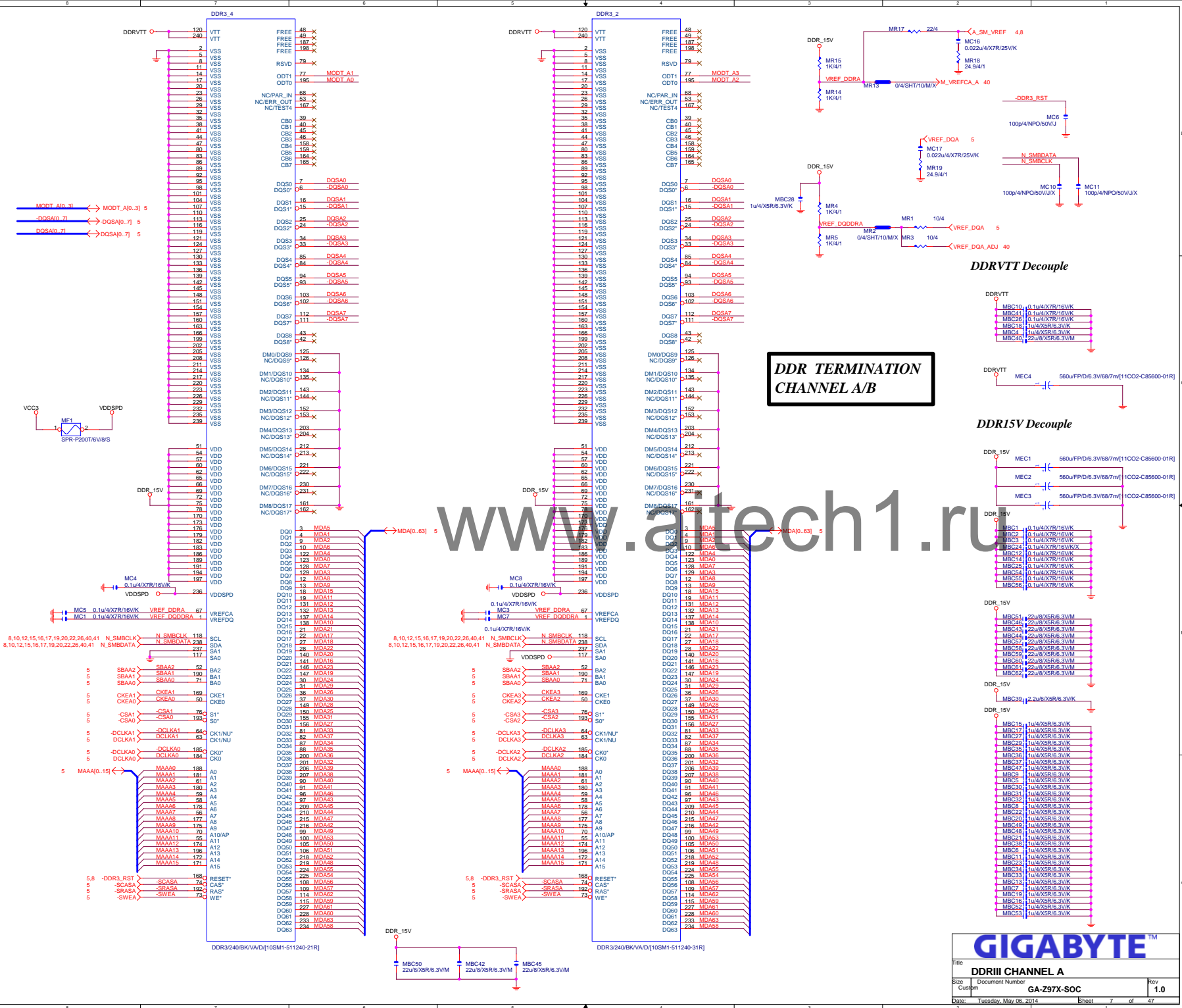
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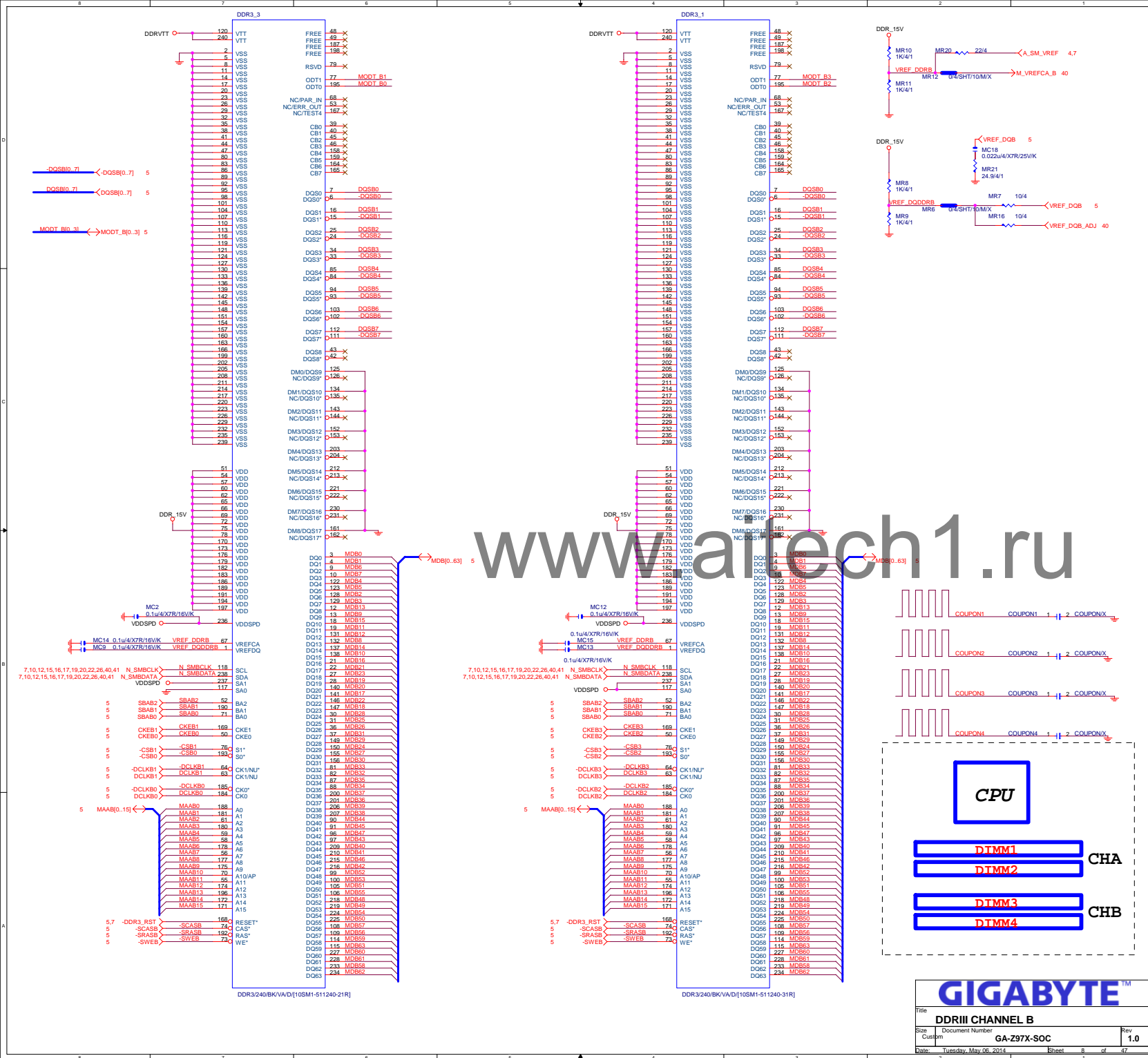
DDR TERMINATION CHANNEL A/B

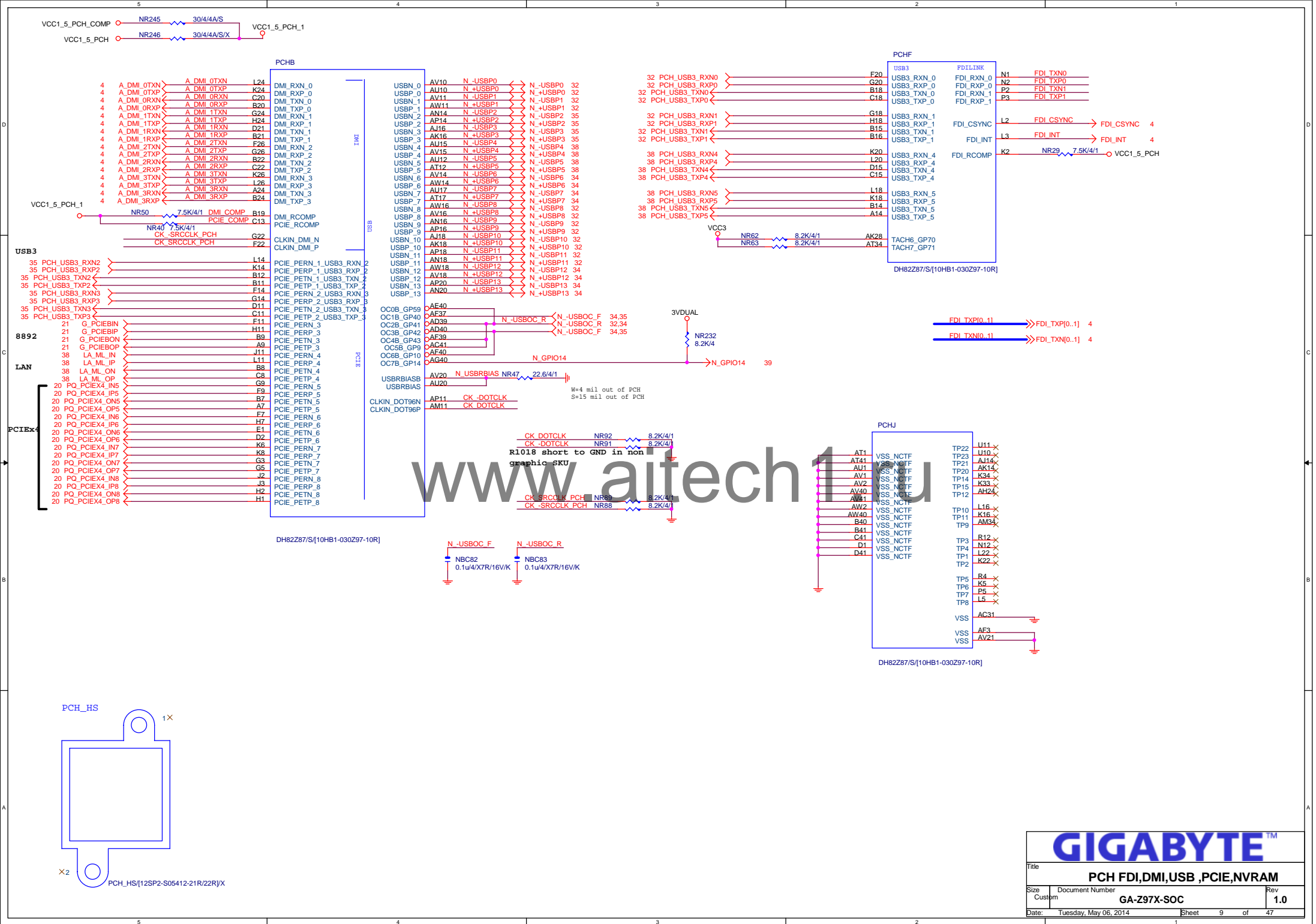
DDRVT Decouple

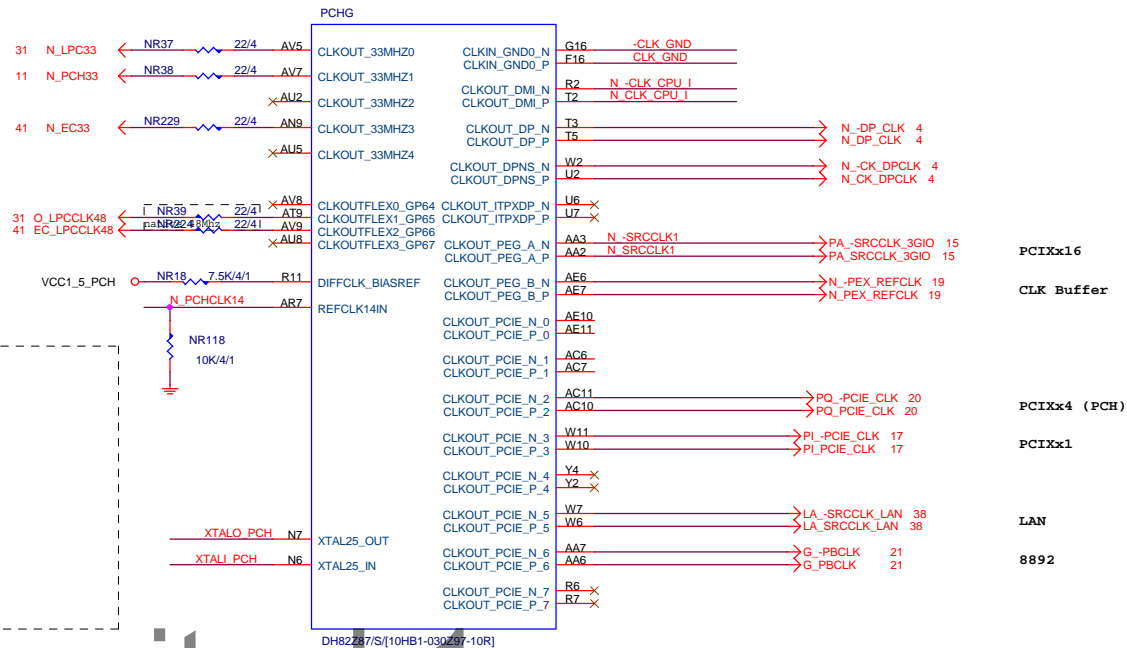
DDR15V Decouple

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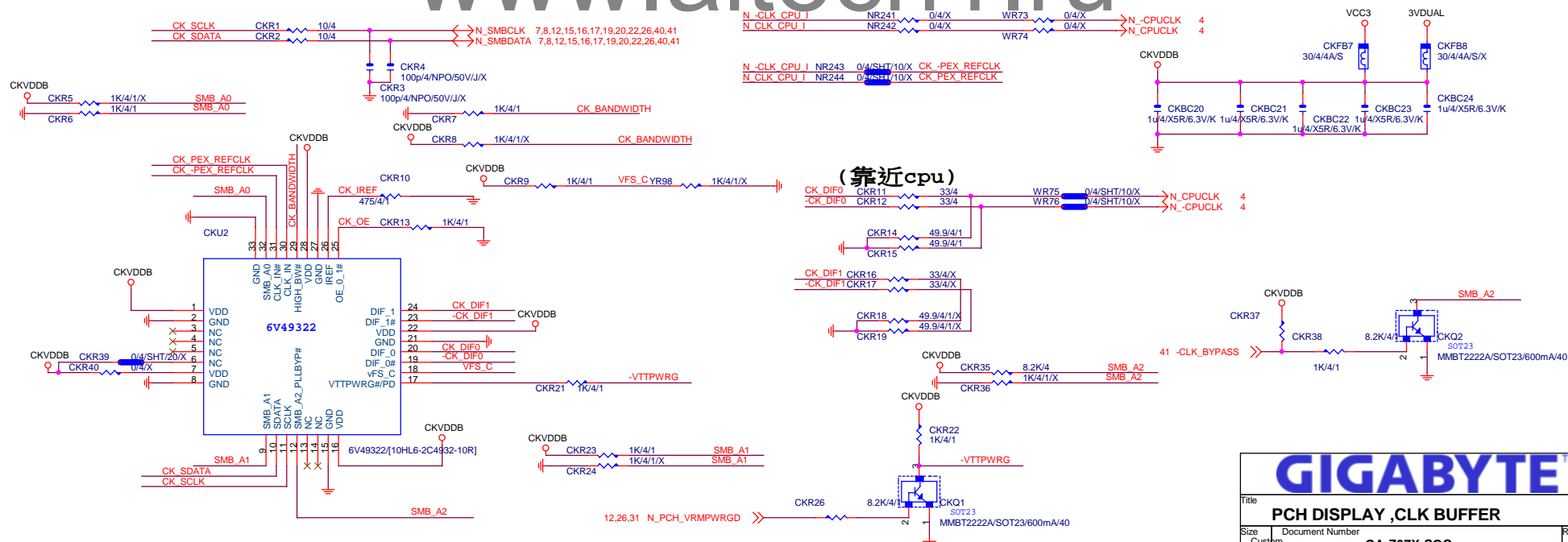
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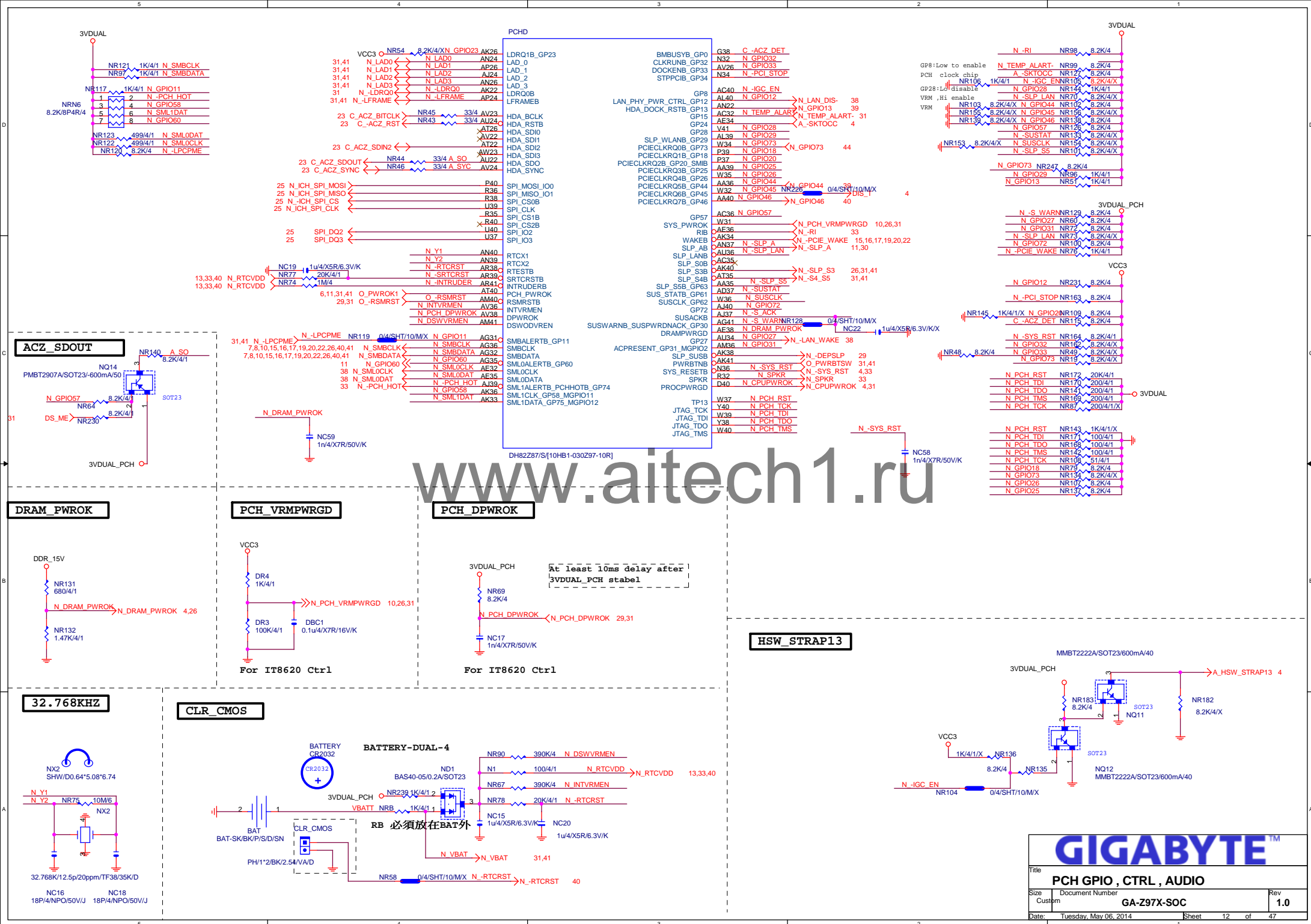






X'TAL 25MHz須參考GND
CRYSTAL/TRACE
週邊不要有訊號,VIA靠近
走線遠離其他40mil以上





www.aitech.ru

+12 protect
short-wire test

PCIE16:16/5/5/16

PA_EXP_RXP0_15] >> PA_EXP_RXP0[0..15] 4,18
PA_EXP_RXN0_15] >> PA_EXP_RXN0[0..15] 4,18
PA_EXP_TXP0_15] >> PA_EXP_TXP0[0..15] 4,18
PA_EXP_TXN0_15] >> PA_EXP_TXN0[0..15] 4,18

PA_EXP_TXP0	PAC5	0.22u4/X5R/6.3V/K	PA_EXP_TXP0 C
PA_EXP_TXN0	PAC4	0.22u4/X5R/6.3V/K	PA_EXP_TXN0 C
PA_EXP_TXP1	PAC6	0.22u4/X5R/6.3V/K	PA_EXP_TXP1 C
PA_EXP_TXN1	PAC7	0.22u4/X5R/6.3V/K	PA_EXP_TXN1 C
PA_EXP_TXP2	PAC8	0.22u4/X5R/6.3V/K	PA_EXP_TXP2 C
PA_EXP_TXN2	PAC9	0.22u4/X5R/6.3V/K	PA_EXP_TXN2 C
PA_EXP_TXP3	PAC10	0.22u4/X5R/6.3V/K	PA_EXP_TXP3 C
PA_EXP_TXN3	PAC11	0.22u4/X5R/6.3V/K	PA_EXP_TXN3 C
PA_EXP_TXP4	PAC12	0.22u4/X5R/6.3V/K	PA_EXP_TXP4 C
PA_EXP_TXN4	PAC13	0.22u4/X5R/6.3V/K	PA_EXP_TXN4 C
PA_EXP_TXP5	PAC14	0.22u4/X5R/6.3V/K	PA_EXP_TXP5 C
PA_EXP_TXN5	PAC15	0.22u4/X5R/6.3V/K	PA_EXP_TXN5 C
PA_EXP_TXP6	PAC16	0.22u4/X5R/6.3V/K	PA_EXP_TXP6 C
PA_EXP_TXN6	PAC17	0.22u4/X5R/6.3V/K	PA_EXP_TXN6 C
PA_EXP_TXP7	PAC18	0.22u4/X5R/6.3V/K	PA_EXP_TXP7 C
PA_EXP_TXN7	PAC19	0.22u4/X5R/6.3V/K	PA_EXP_TXN7 C
PA_EXP_SW_TXP8	PAC21	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP8 C
PA_EXP_SW_TXN8	PAC20	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN8 C
PA_EXP_SW_TXP9	PAC22	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP9 C
PA_EXP_SW_TXN9	PAC23	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN9 C
PA_EXP_SW_TXP10	PAC24	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP10 C
PA_EXP_SW_TXN10	PAC25	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN10 C
PA_EXP_SW_TXP11	PAC26	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP11 C
PA_EXP_SW_TXN11	PAC27	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN11 C
PA_EXP_SW_TXP12	PAC28	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP12 C
PA_EXP_SW_TXN12	PAC29	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN12 C
PA_EXP_SW_TXP13	PAC30	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP13 C
PA_EXP_SW_TXN13	PAC31	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN13 C
PA_EXP_SW_TXP14	PAC32	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP14 C
PA_EXP_SW_TXN14	PAC33	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN14 C
PA_EXP_SW_TXP15	PAC34	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXP15 C
PA_EXP_SW_TXN15	PAC35	0.22u4/X5R/6.3V/K	PA_EXP_SW_TXN15 C

PA_EXP_SW_RXP8_15] >> PA_EXP_SW_RXP8[8..15] 18
PA_EXP_SW_RXN8_15] >> PA_EXP_SW_RXN8[8..15] 18
PA_EXP_SW_TXP8_15] >> PA_EXP_SW_TXP8[8..15] 18
PA_EXP_SW_TXN8_15] >> PA_EXP_SW_TXN8[8..15] 18

PCI-E REV:1.1--> 2.5GHZ

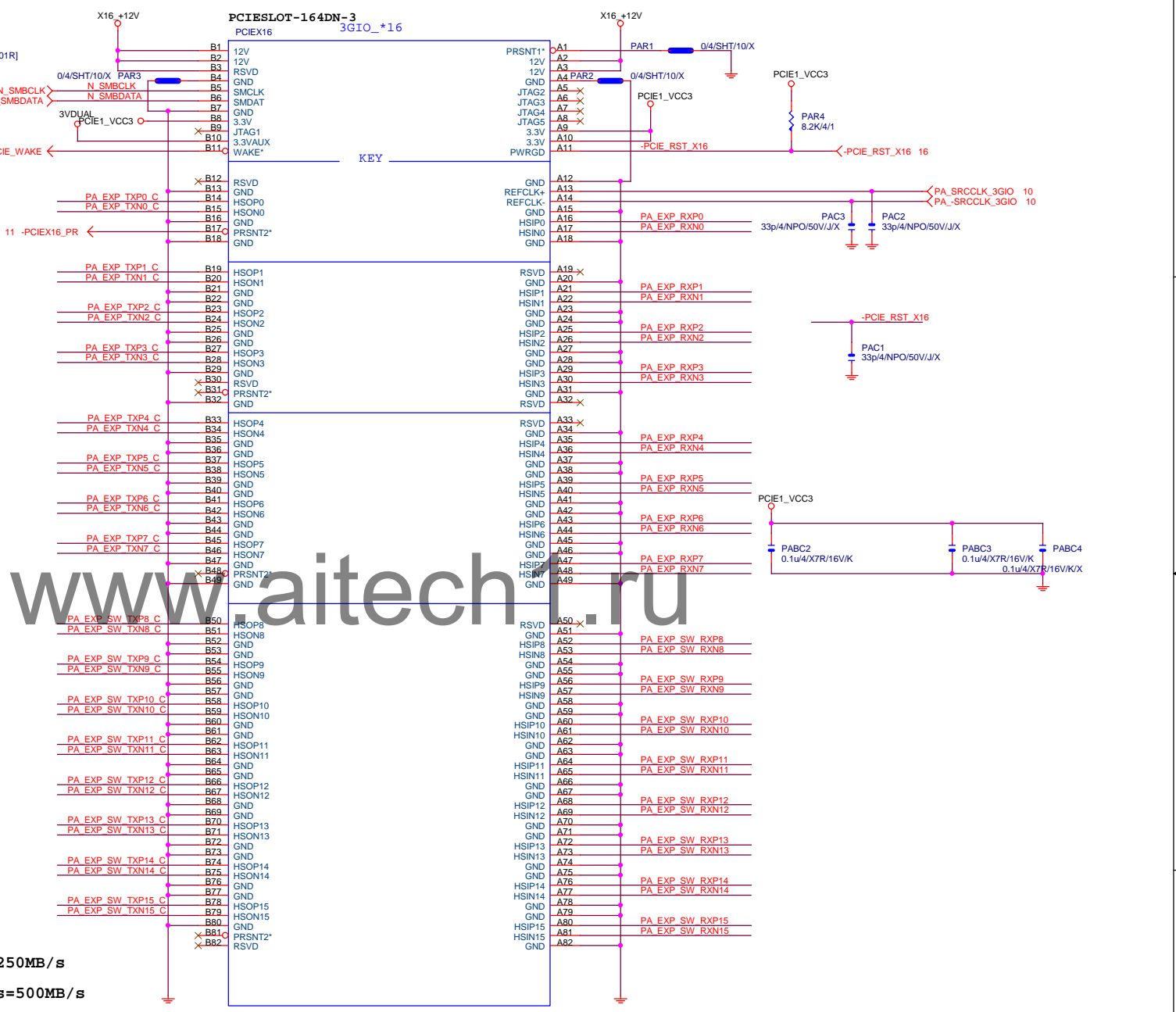
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ



PCI-E/16x-164P/BK/RIGHT PUSH-[11AC1-023164-62R]

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Title
PCI EXPRESS * 16

Size
Custom

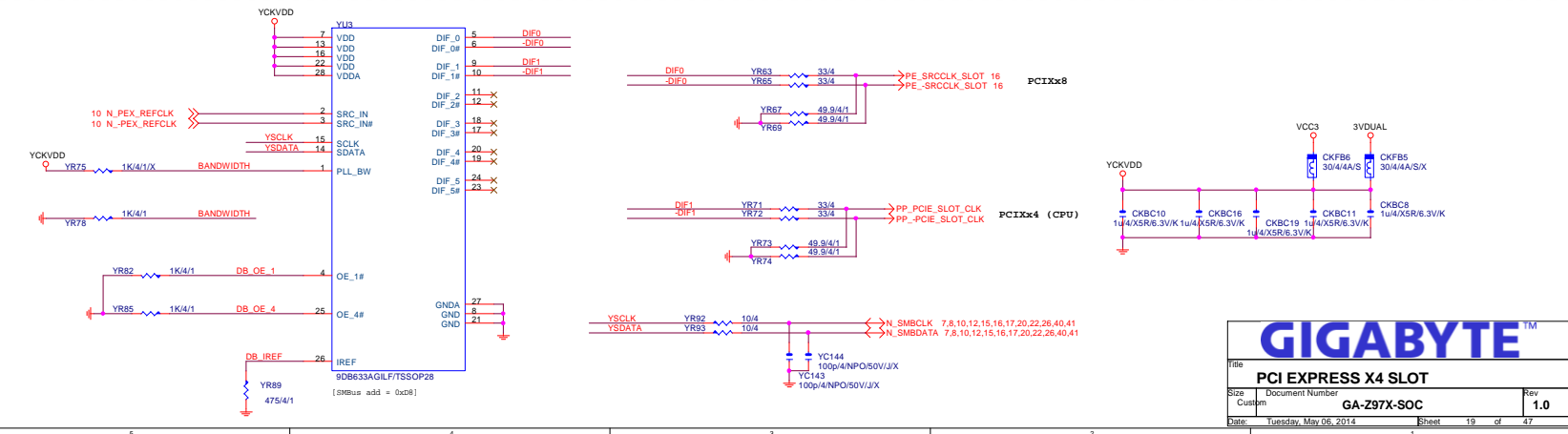
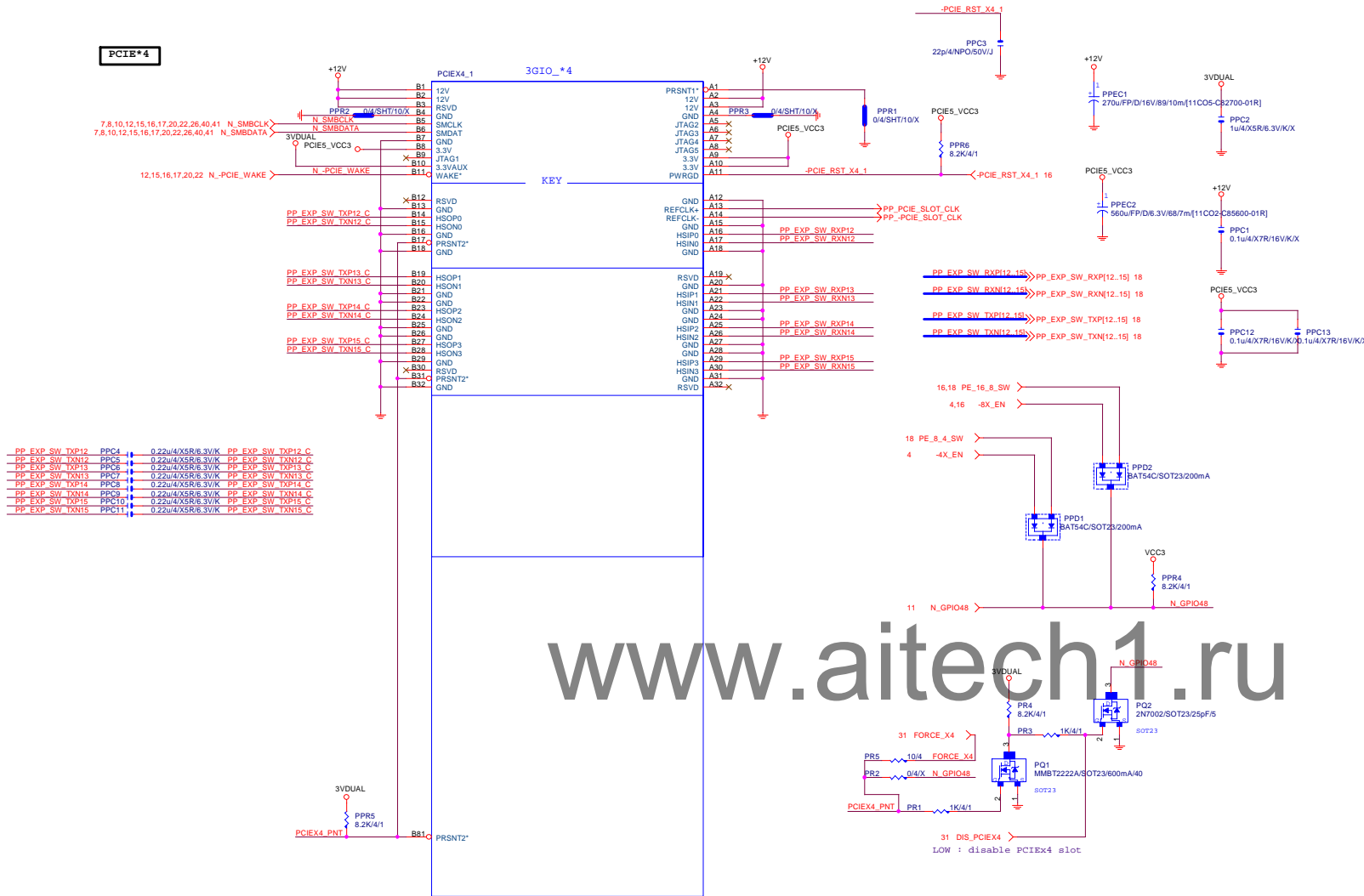
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GA-Z97X-SOC

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1.0

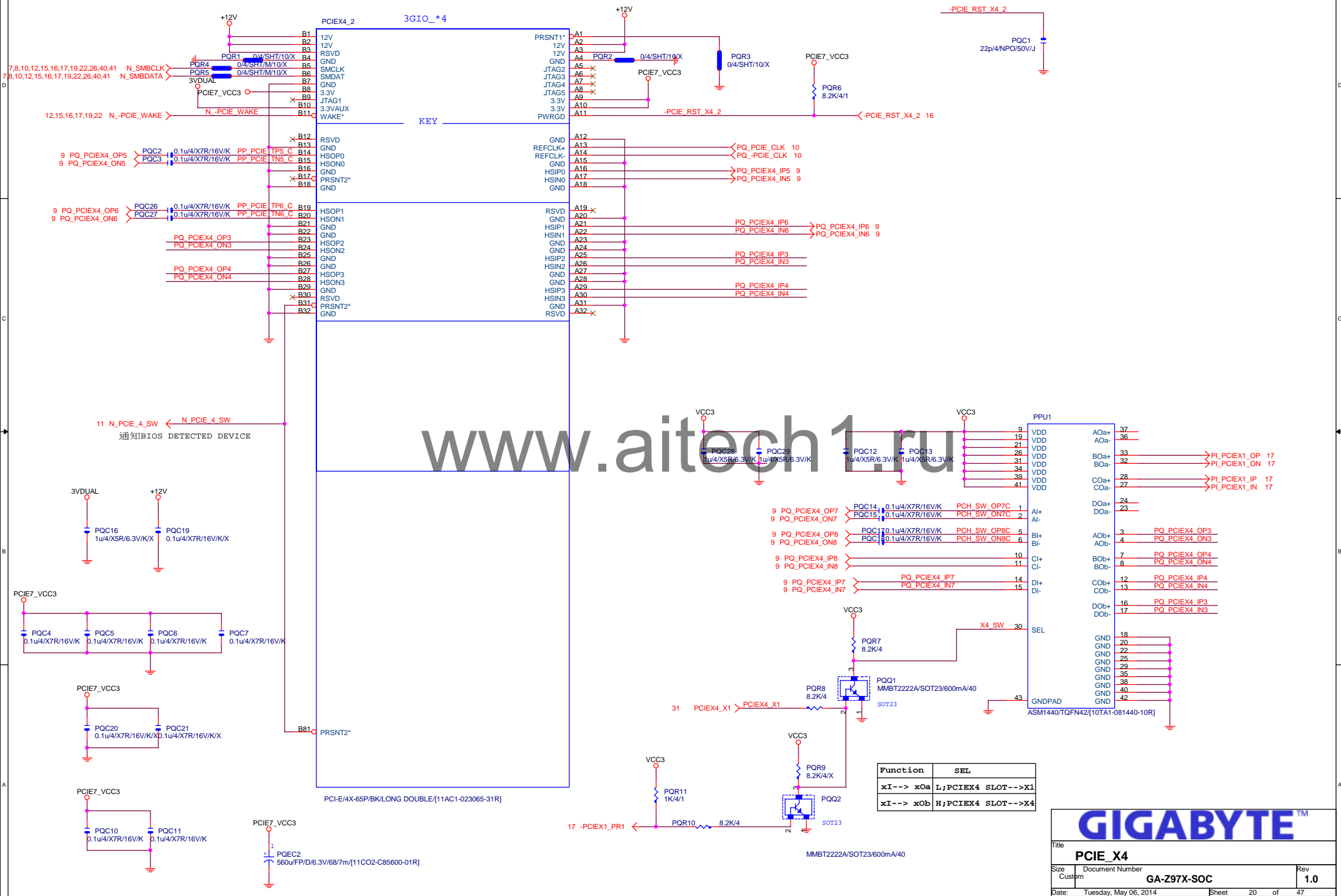
Date
Tuesday, May 06, 2014

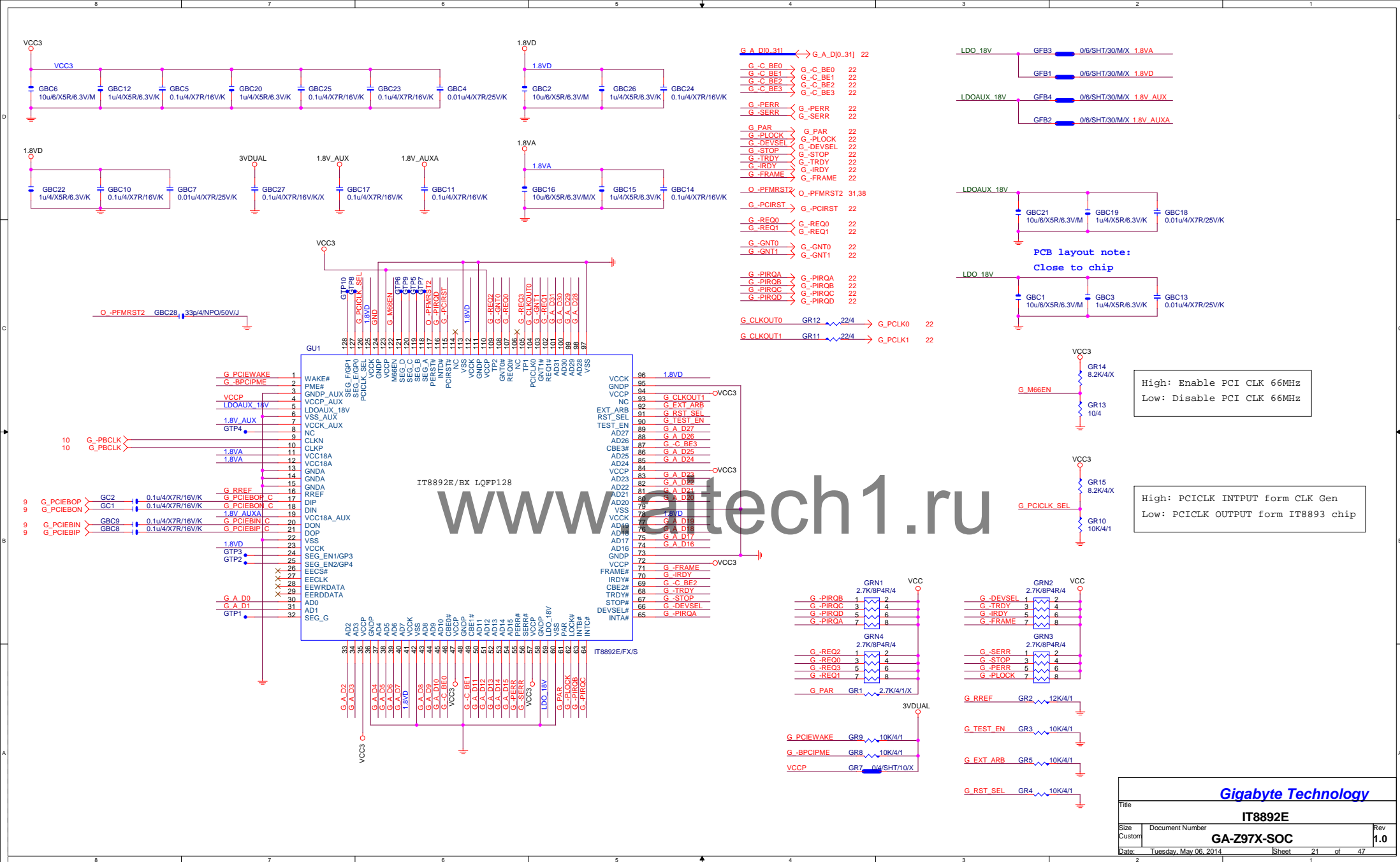
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15

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47



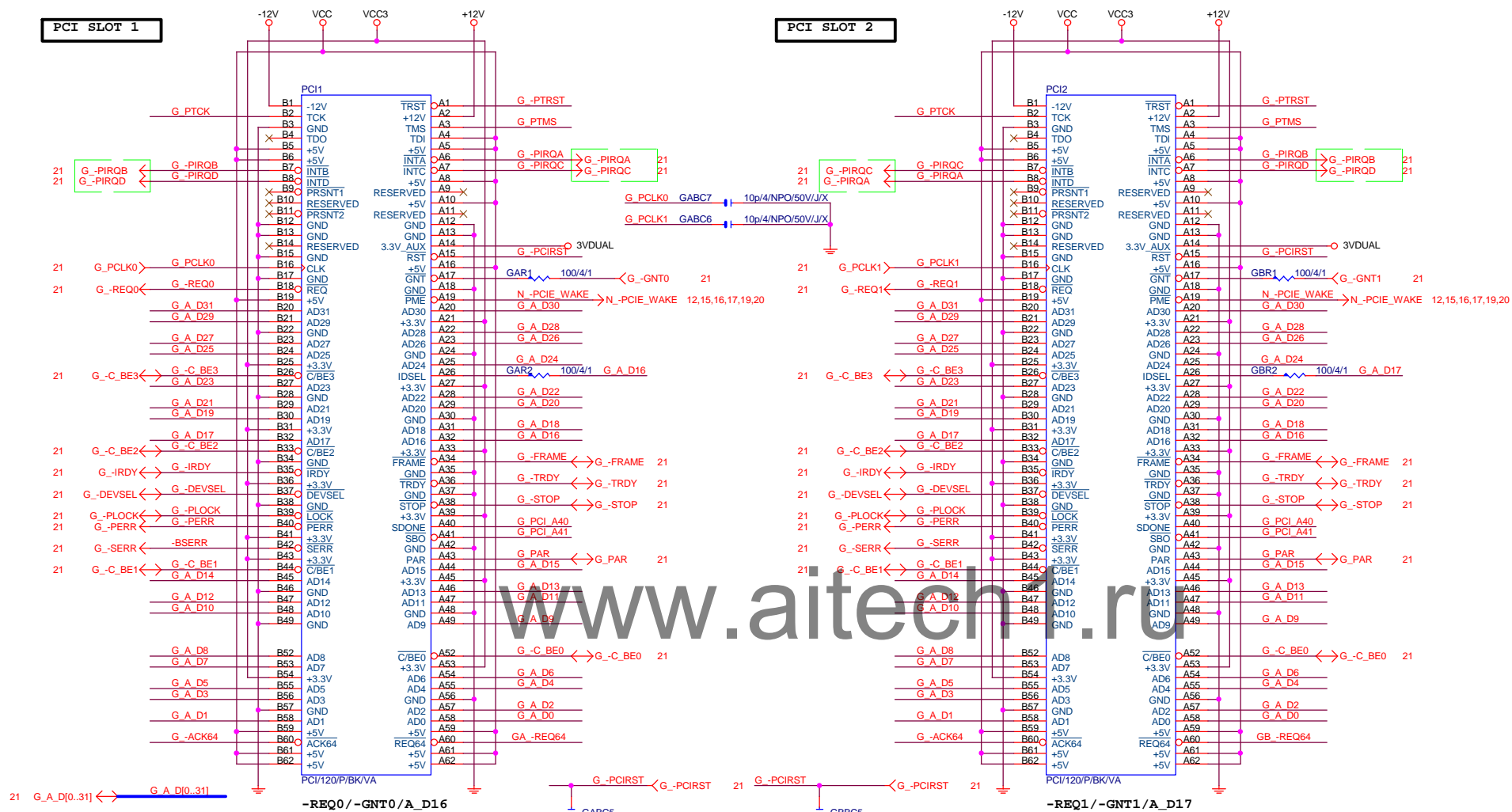
PCIE*4





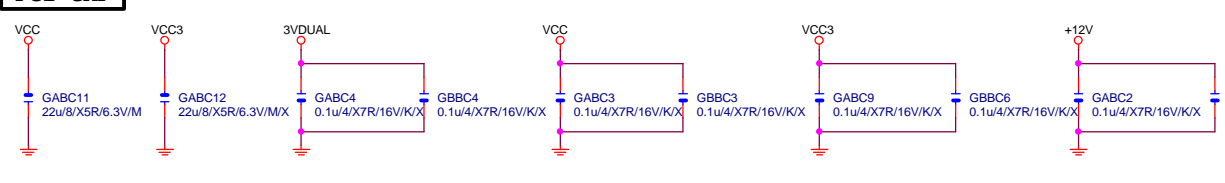
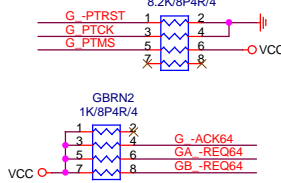
PCI SLOT 1

PCI SLOT 2



PCI PU

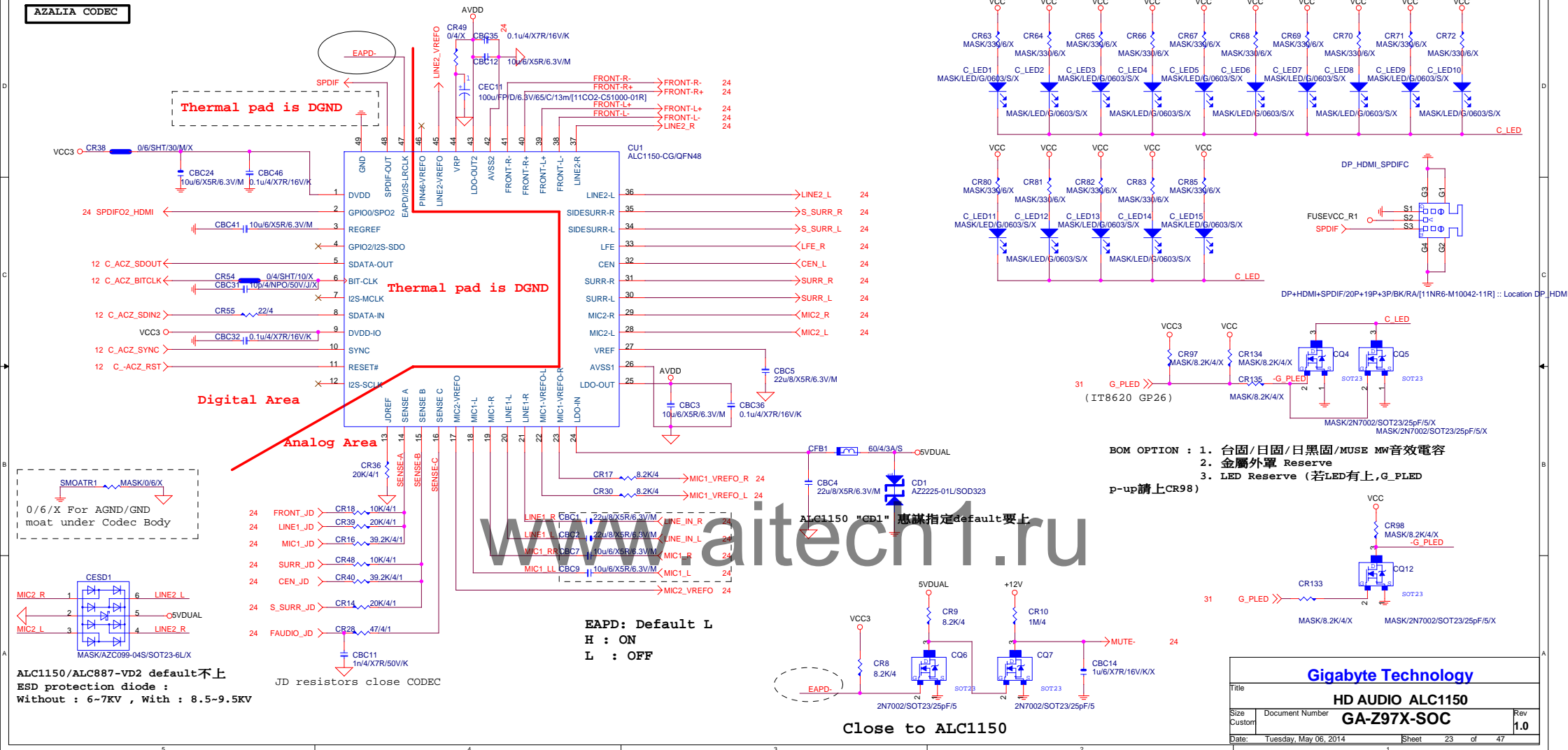
PCI CAP

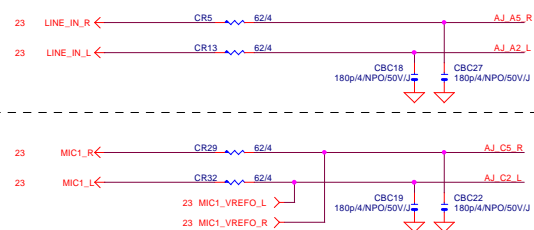
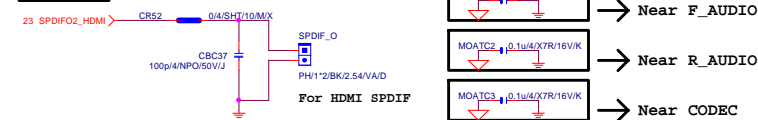
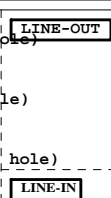


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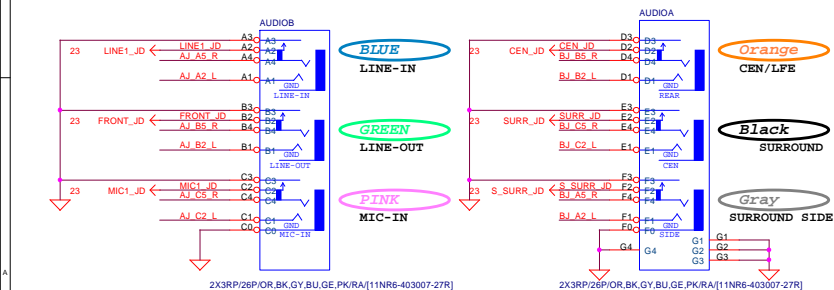
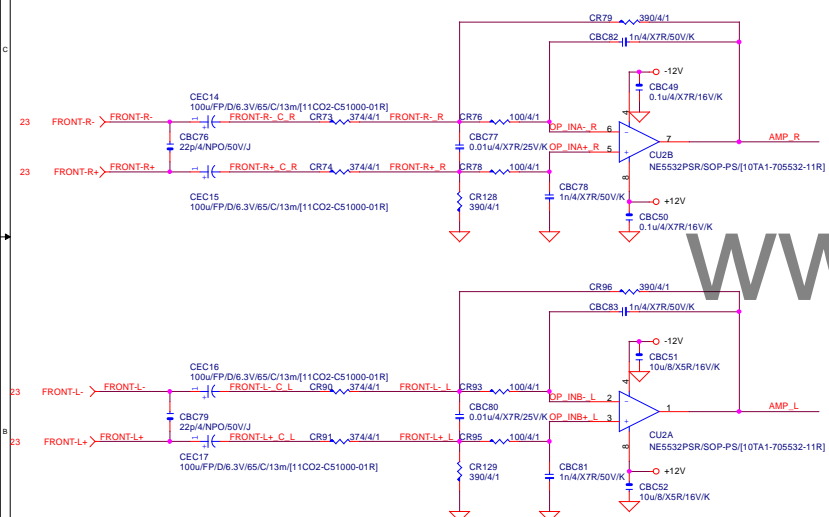
PCI SLOT 1&2

Size	Document Number	Rev
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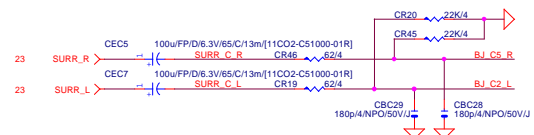




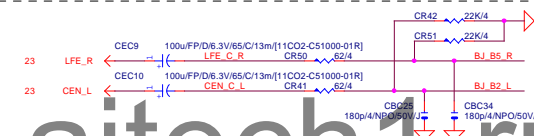
Differential to Single-End AMPLIFIED



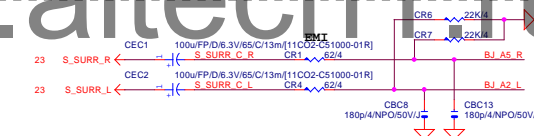
SURROUND



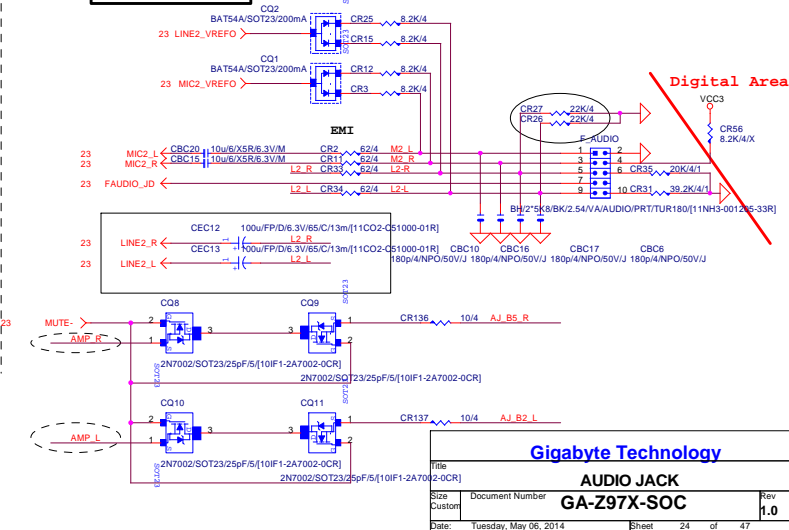
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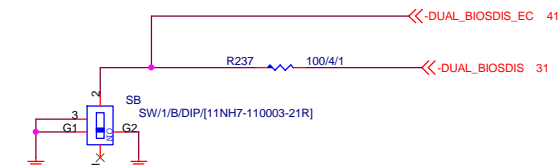
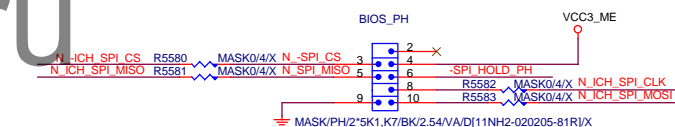
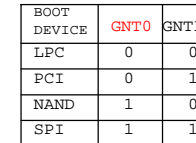


SURRBACK



AZALIA FRONT PANEL





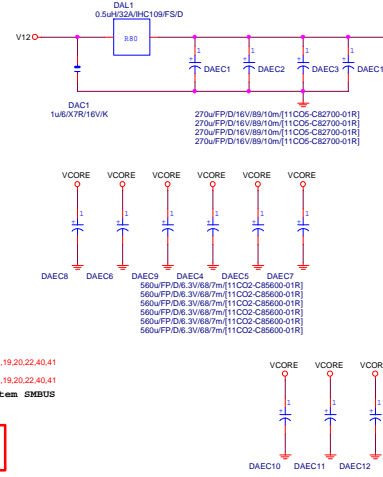
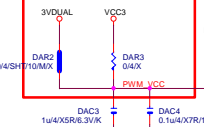
1	Main_BIOS
2	Backup_BIOS

Value need check with Vendor

should be routed as differential pair, 7mil width, 8mil spacing

Close to DDR output inductor

need 0.1amp , check trace width



Debug Port

To system SMBUS

To CPU side SVID Bus

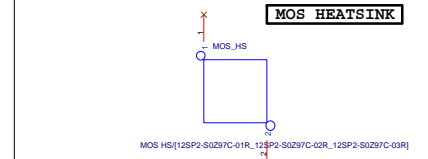
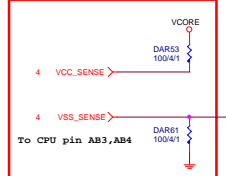
IR3564

OUP/UVP=250mV
OCP=200A
VRHOT=125 Degree
OTP=130 Degree

Value need check with Vendor

should be routed as differential pair, 7mil width, 8mil spacing

Close to Vcore output inductor

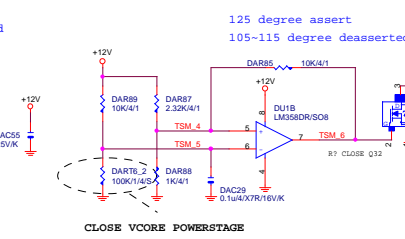
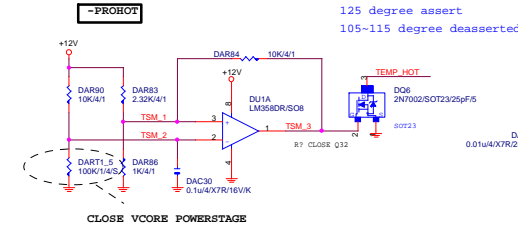
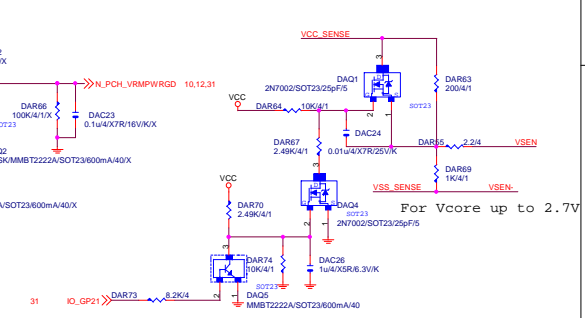


should be routed as differential pair, 7mil width, 8mil spacing

should be routed as differential pair, 7mil width, 8mil spacing

Close to Vcore MOS DD_DQ3

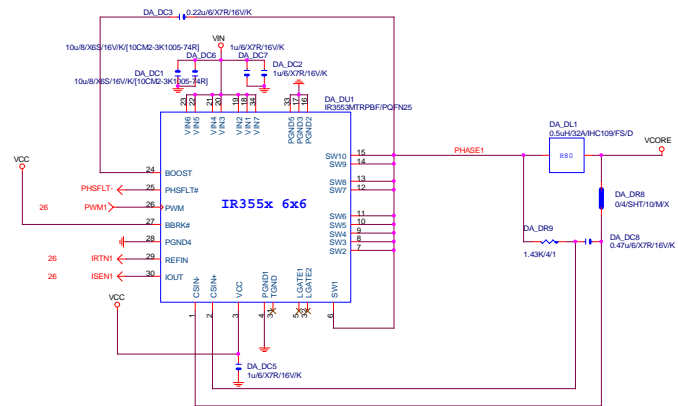
should be routed as differential pair, 7mil width, 8mil spacing



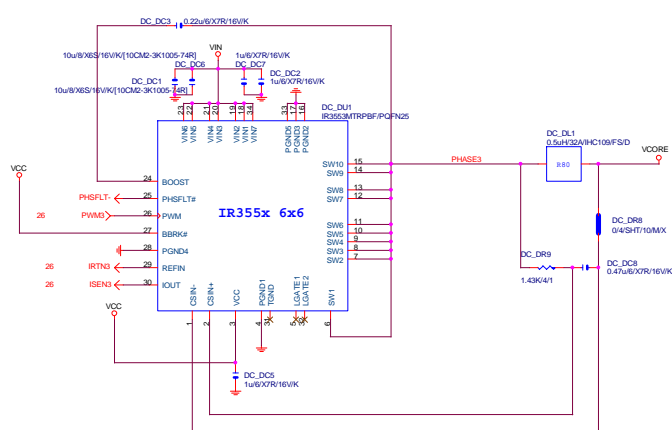
Gigabyte Technology			
File	IR3564A for VR12.5 DT		
Size	Document Number	Rev	
Custom	GA-Z97X-SOC	1.0	
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VCORE

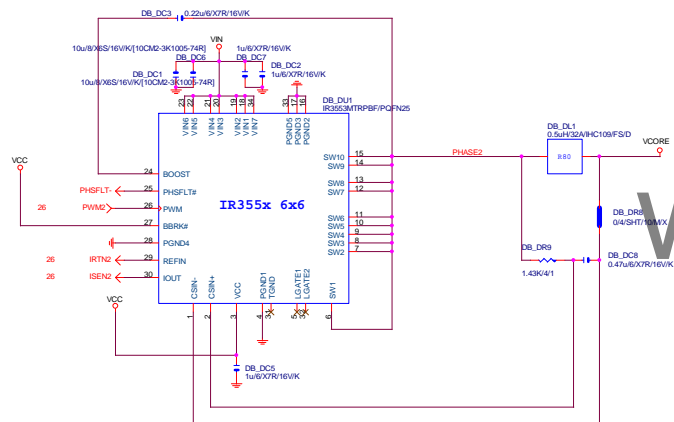
VCORE-PHASE1



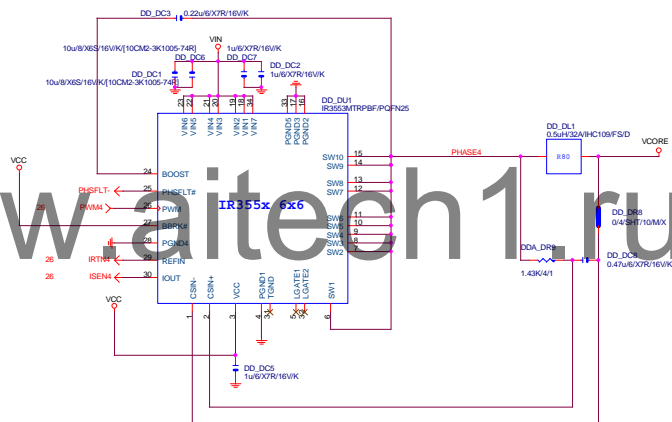
VCORE-PHASE3



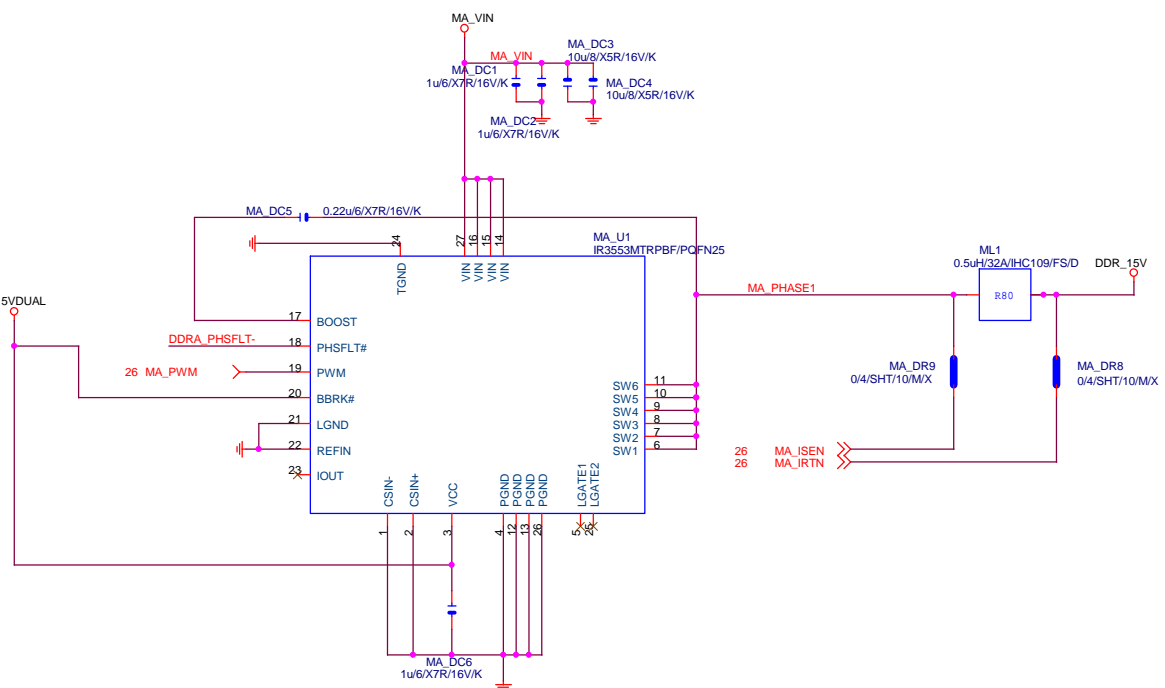
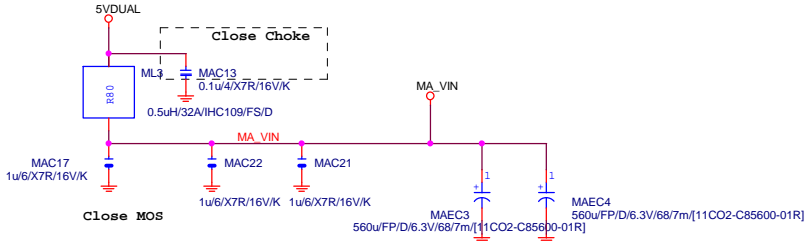
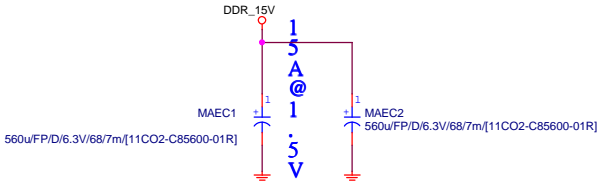
VCORE-PHASE2



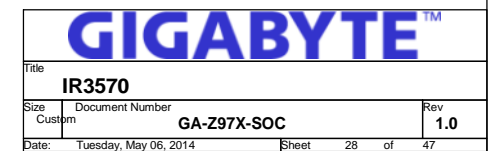
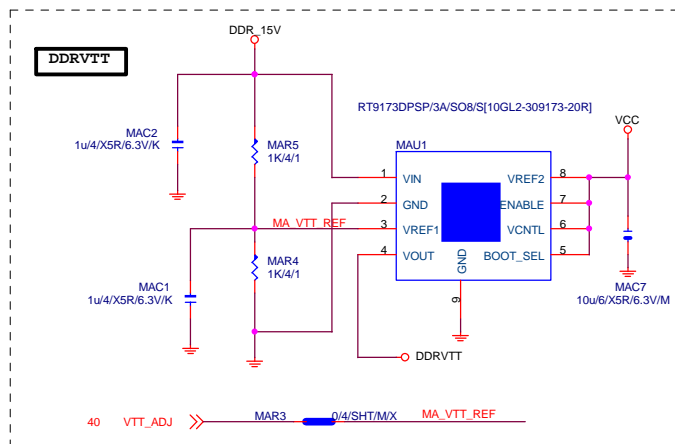
VCORE-PHASE4



DDR_15V

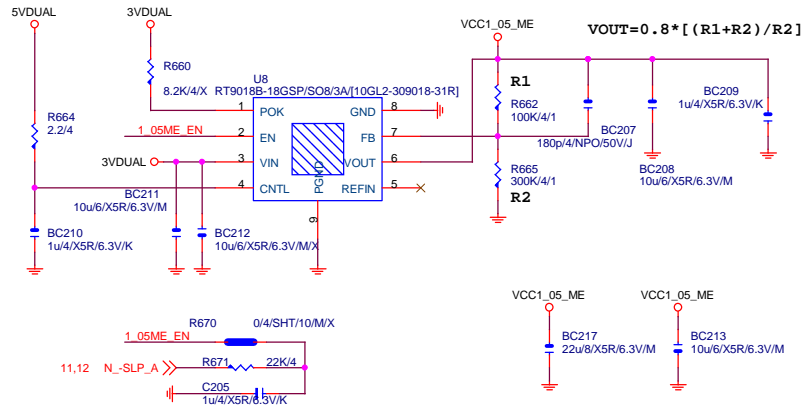


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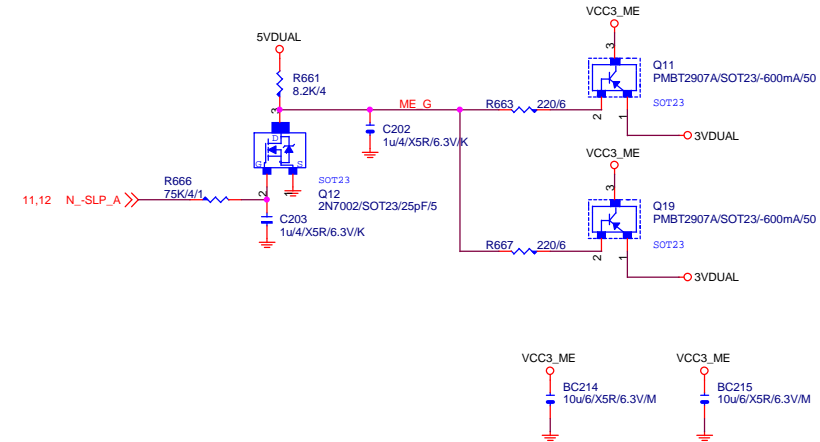


VCC1_05_ME

【技術通報R&D技術通報156】
(RICHTER), (NUVOTON), (EMC) 做共用
PIN7分壓阻值須做修改為100K以上電阻值

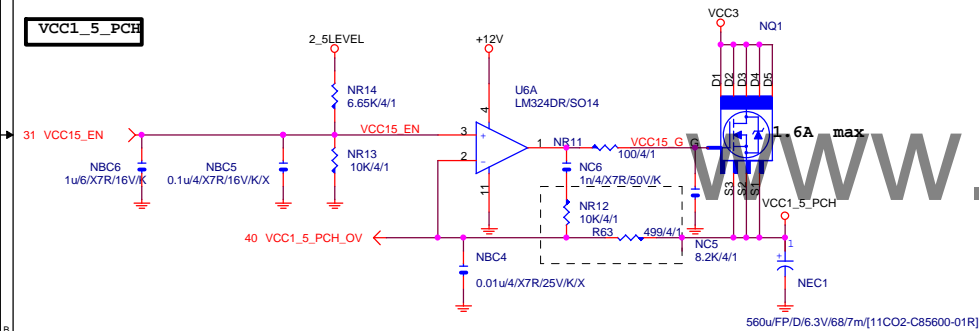


VCC3_ME



VCC1_5_PCH

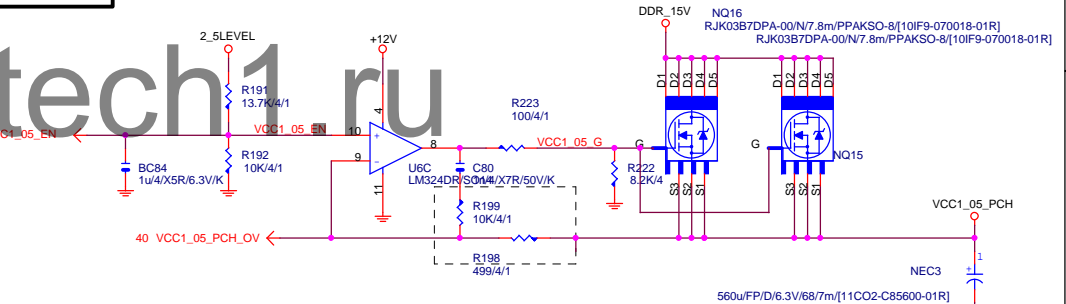
RJK03B7DPA-00/N/7.8m/PPAKSO-8/[10IF9-070018-01R]



Rise/Fall max 50us
Rise:20% - 80%
Fall :2V- 0.8V

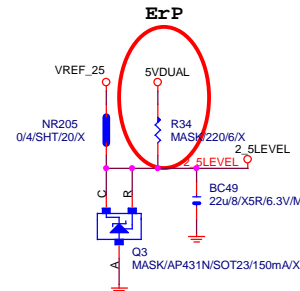
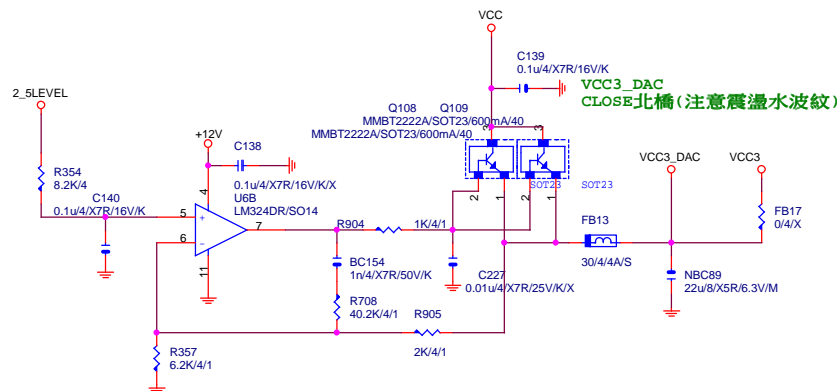
At least 10ms delay after 3VDUAL ready
Pop when PCH & SIO both use 3VDUAL-PCH

VCC1_05_PCH



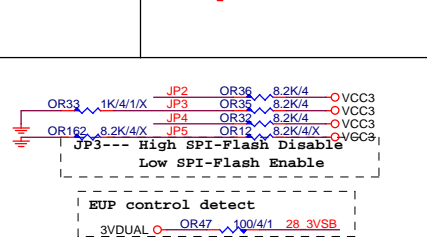
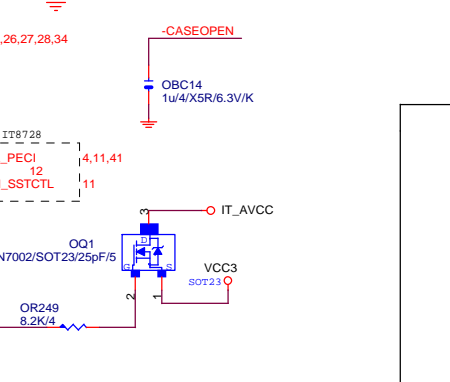
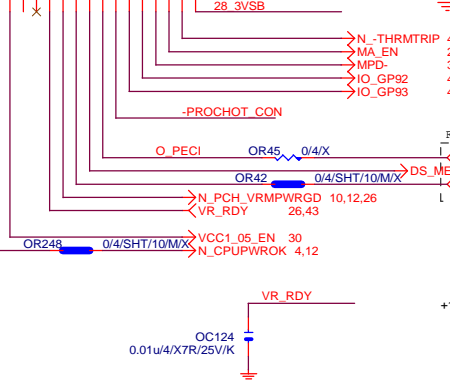
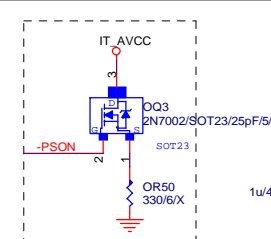
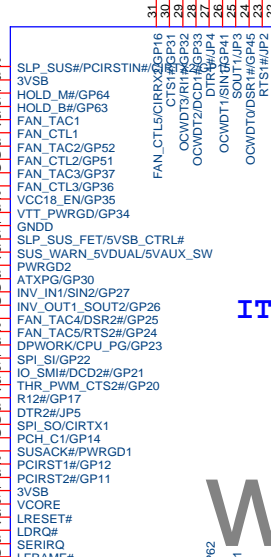
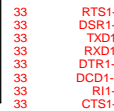
VCC3_DAC

(3.3V/70mA+360uA)



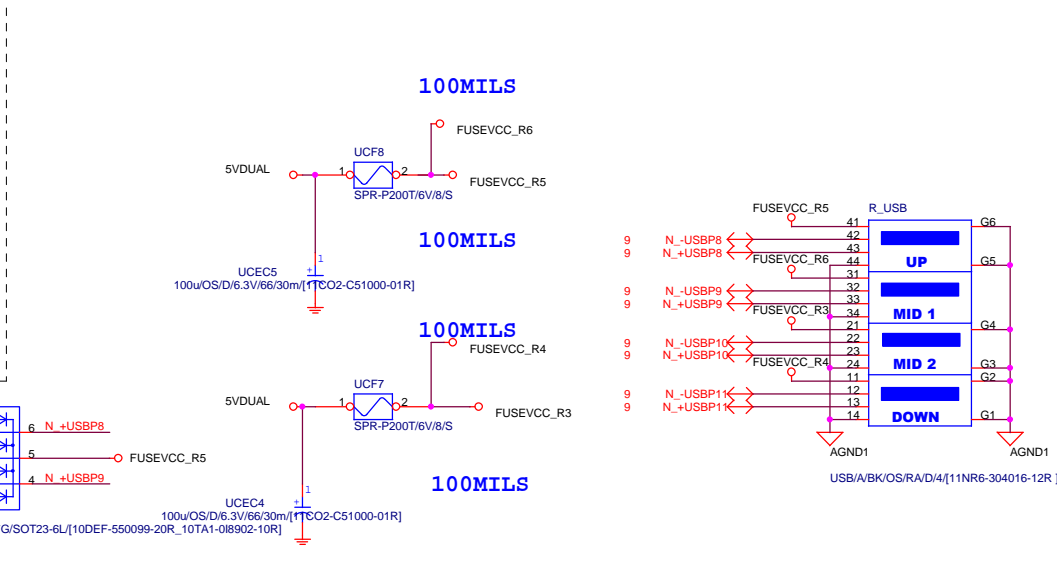
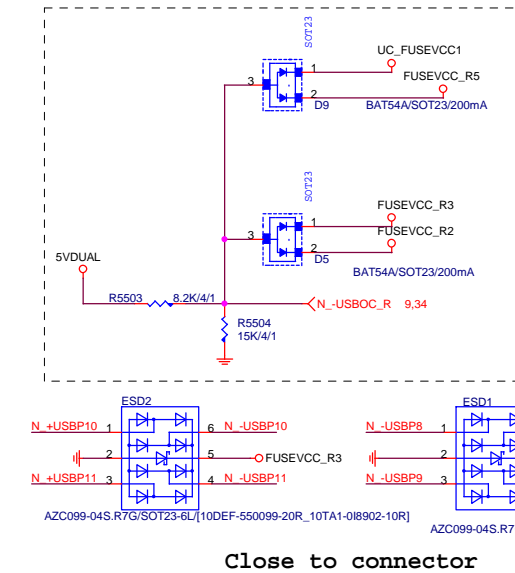
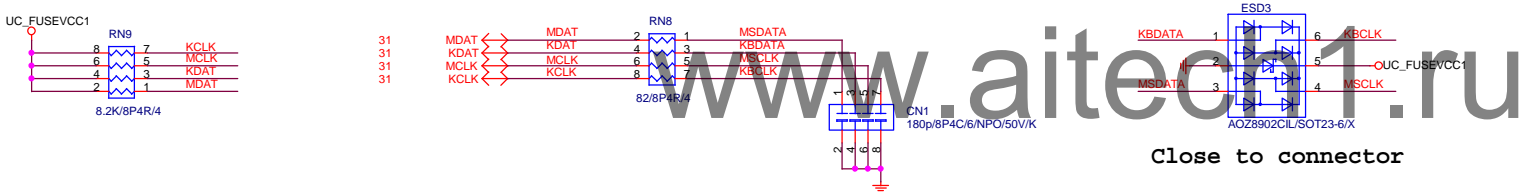
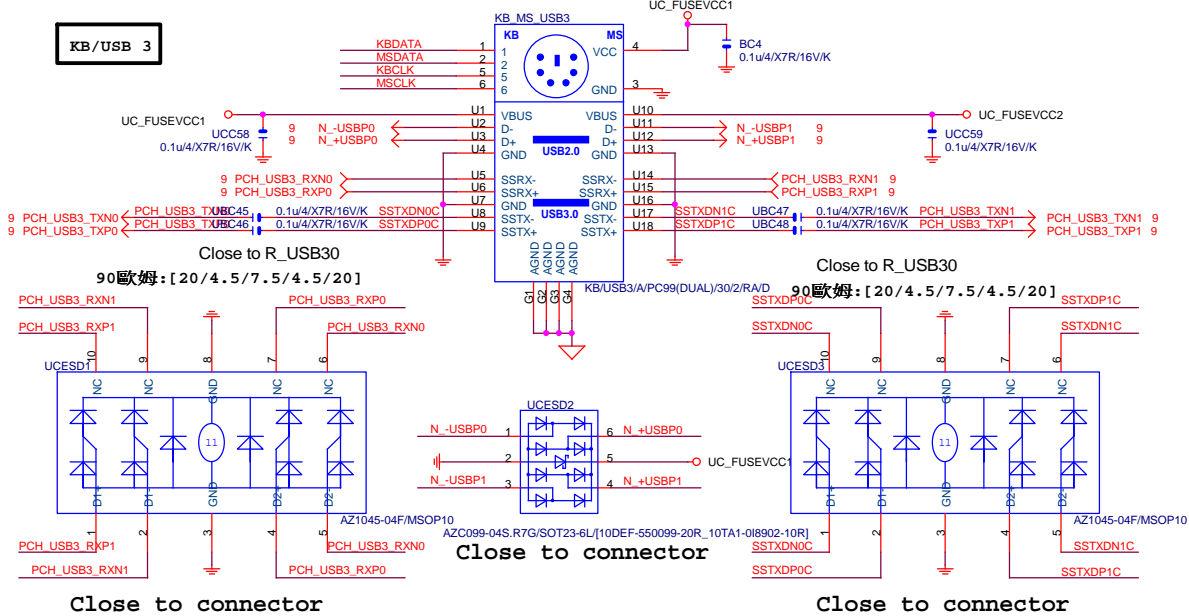
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Title	VCC 1.05 PCH, VCC1.5 PCH, CC3 DAC	
Size	Document Number	Rev
Custom	GA-Z97X-SOC	1.0
Date:	Tuesday, May 06, 2014	Sheet 30 of 47

```
internal_power_pin, max_22nF_cap
```



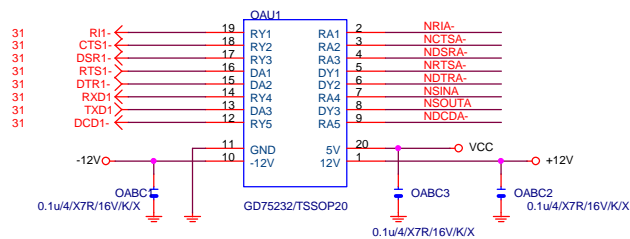
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KB/USB 3

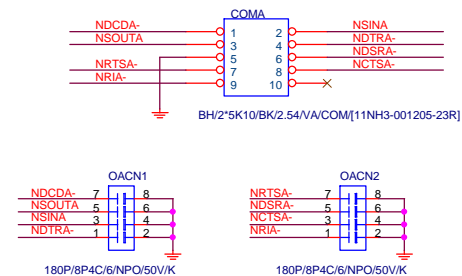
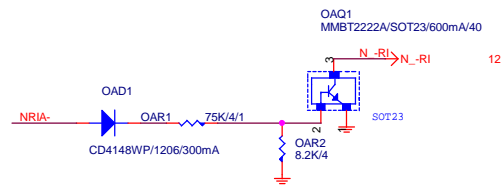


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Size Custom	Document Number GA-Z97X-SOC	Rev 1.0
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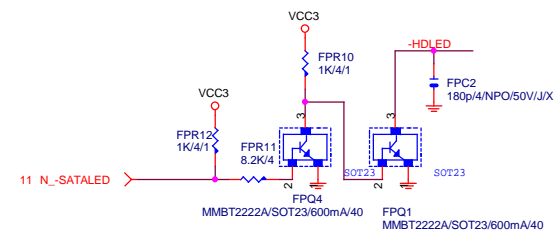
COMA



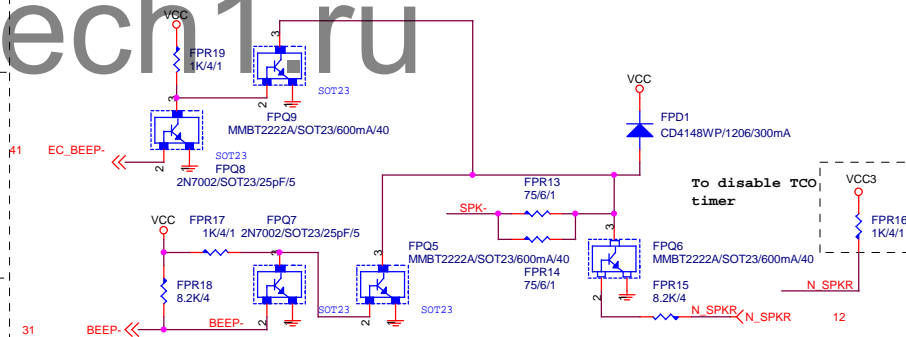
COM RI



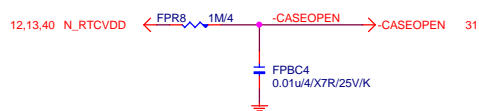
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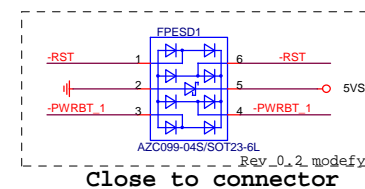
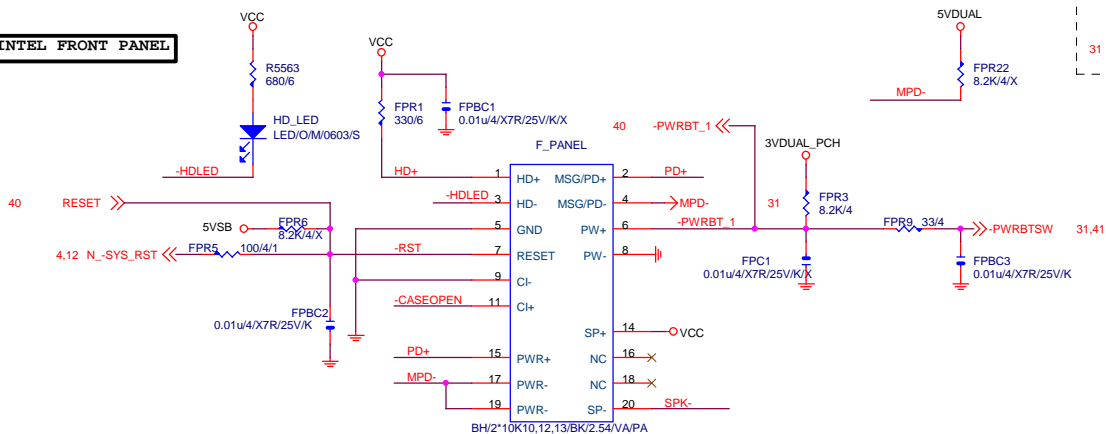
SPKR



CASE OPEN



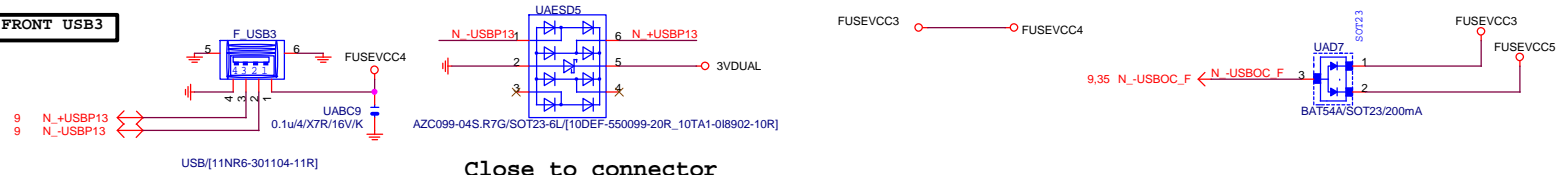
INTEL FRONT PANEL



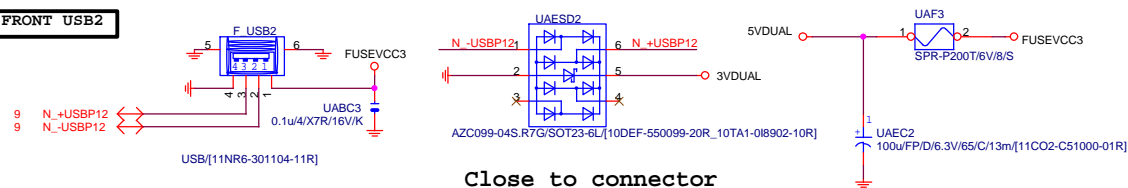
GIGABYTE™

Title			
FP, COM, -PHOT			
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FRONT USB3

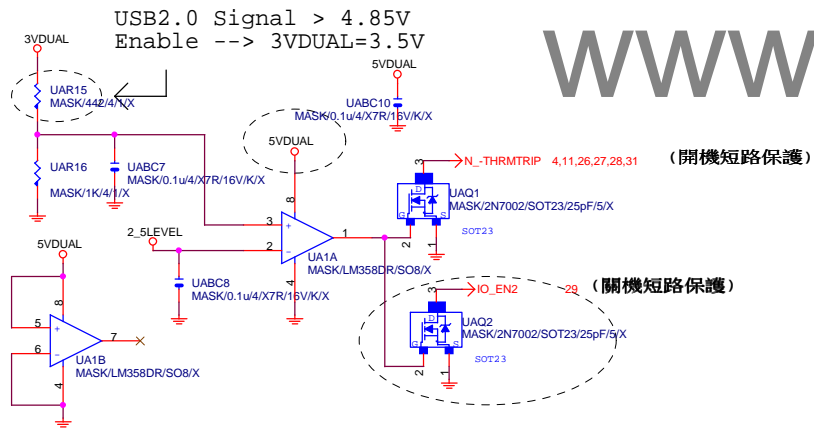


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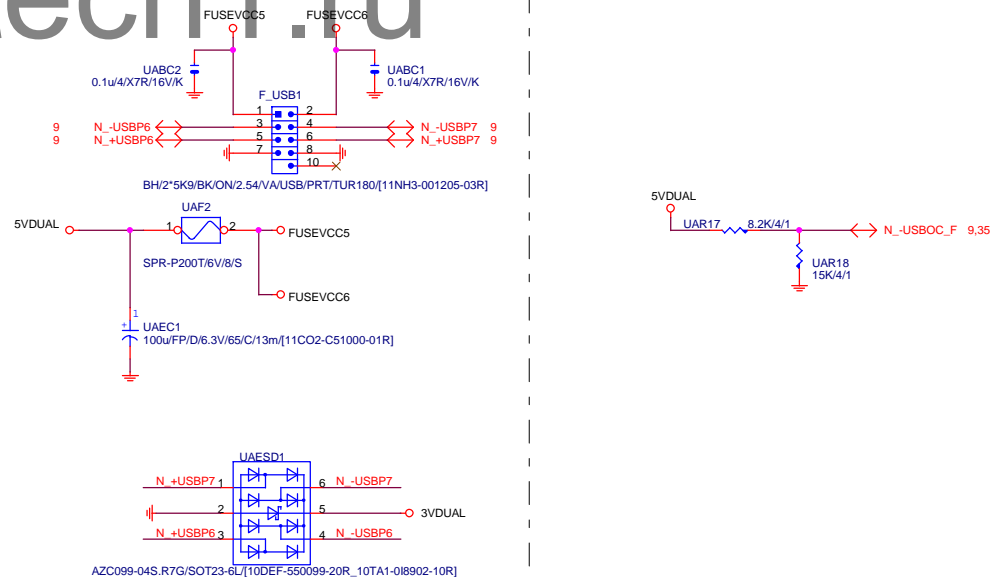


USB2.0 Signal & power short protection

MASK

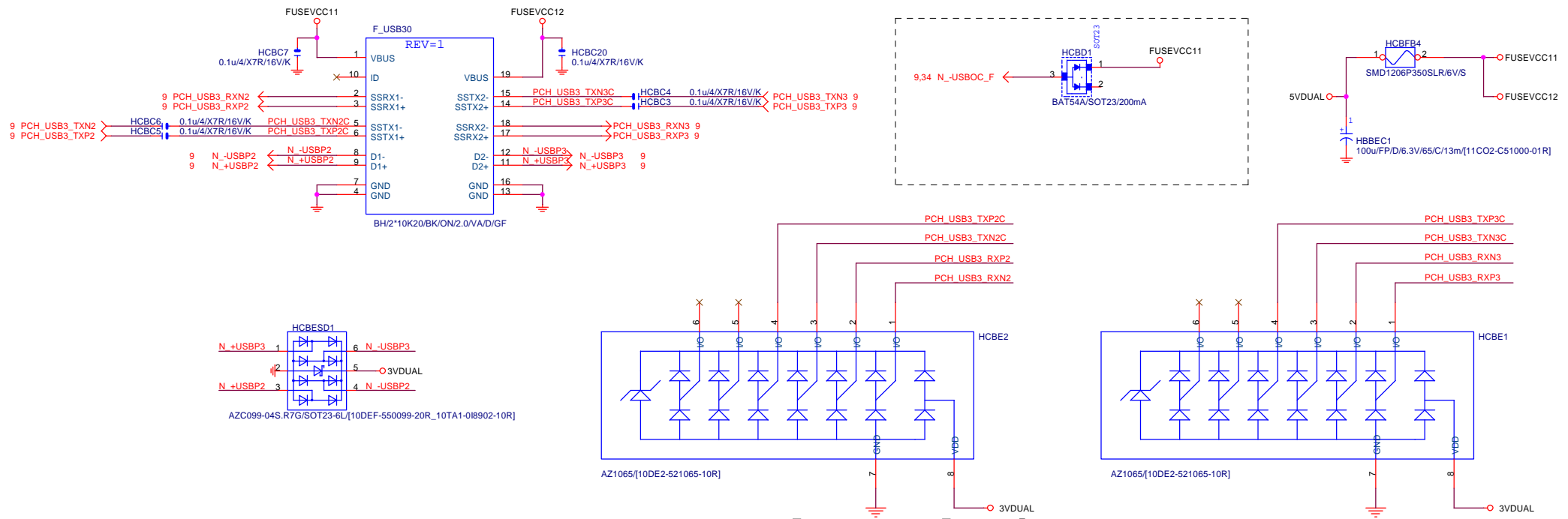


FRONT USB1



GIGABYTE

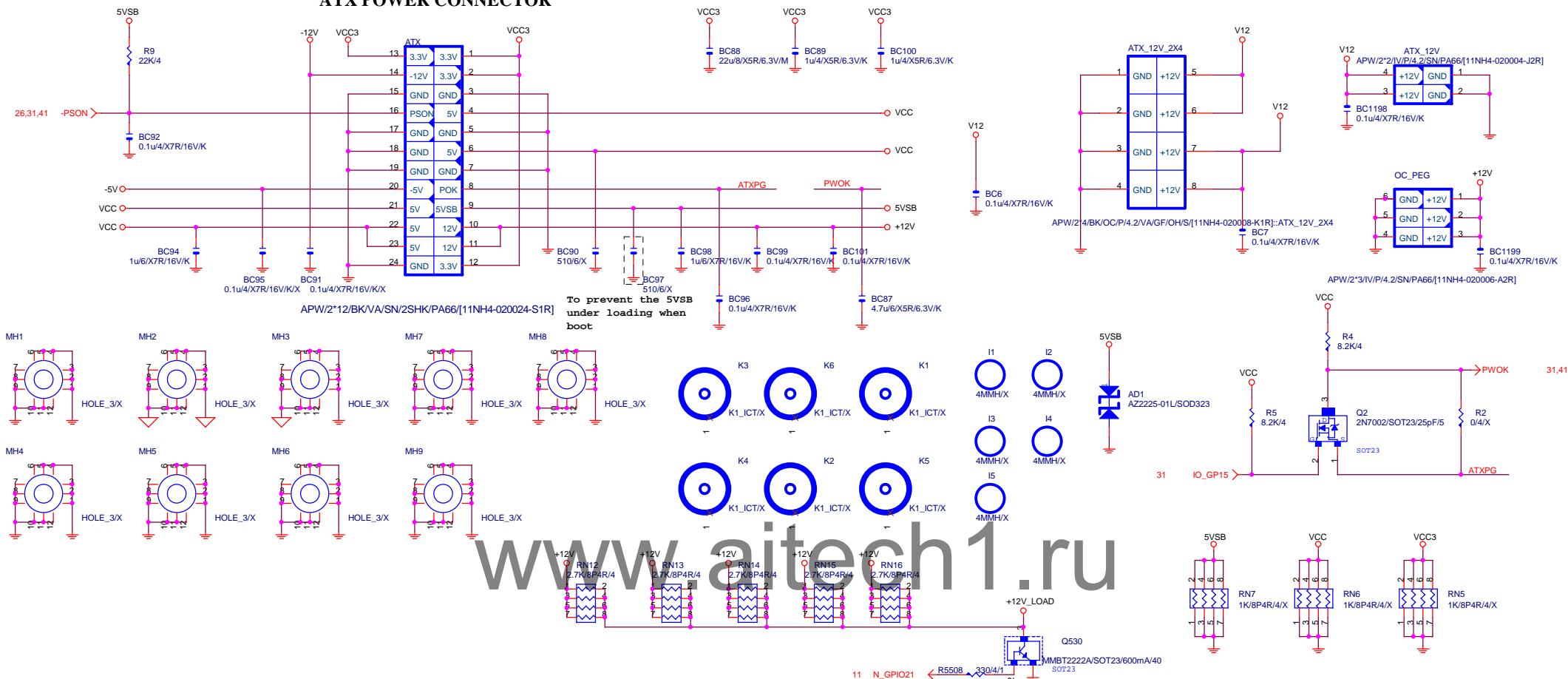
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Size Custom	Document Number GA-Z97X-SOC	Rev 1.0
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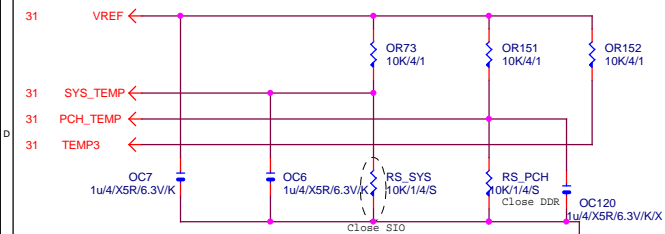
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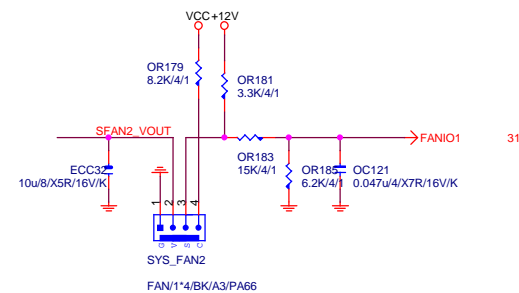
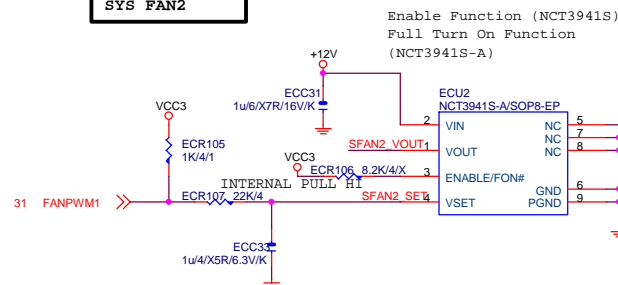
ATX POWER CONNECTOR



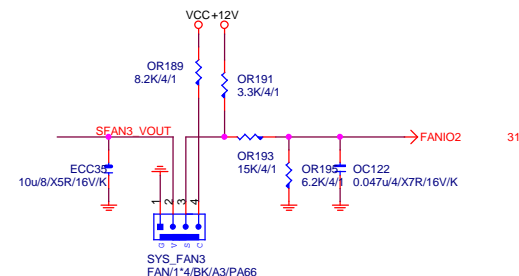
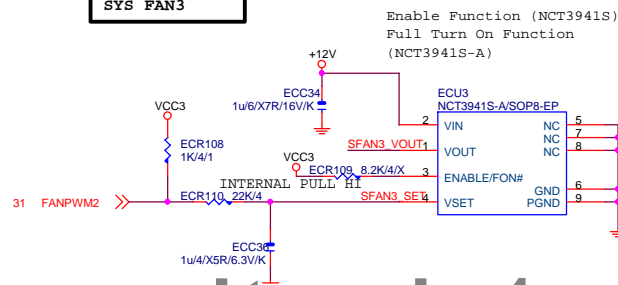
TEMP H/W MONITOR



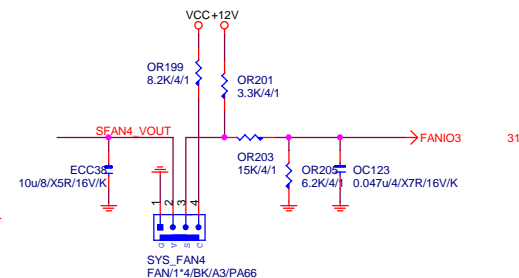
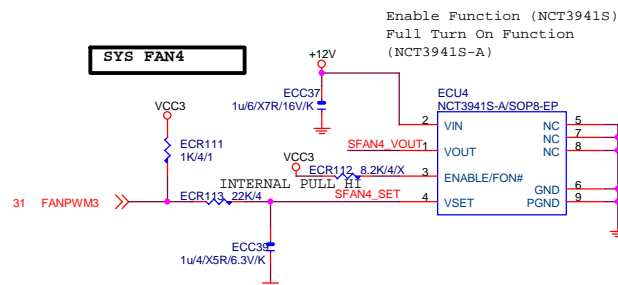
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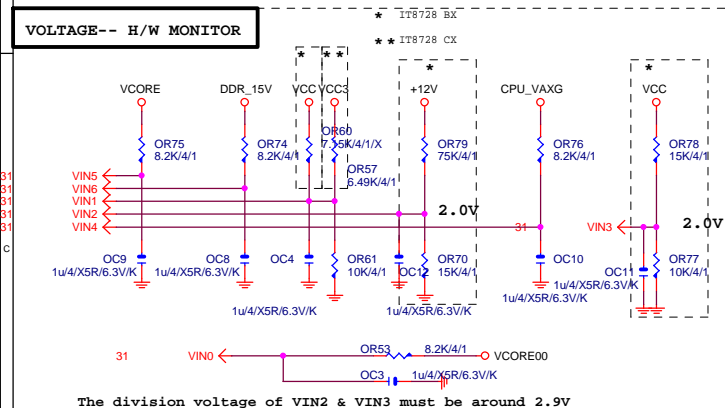
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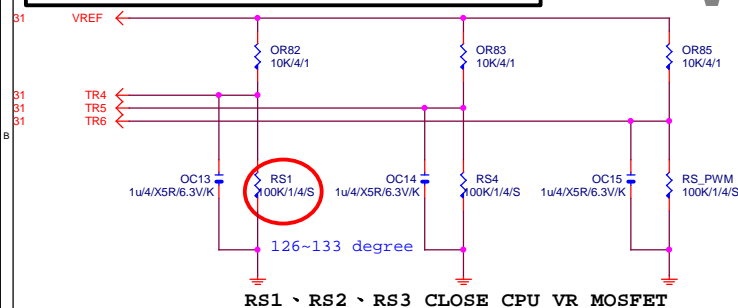
SYS FAN4



VOLTAGE-- H/W MONITOR



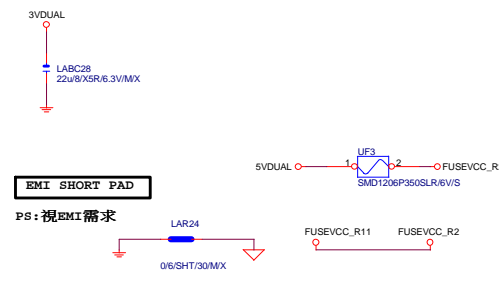
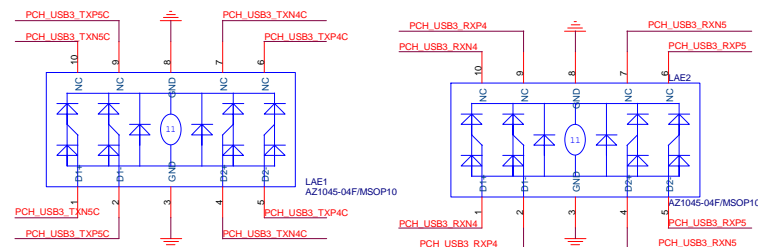
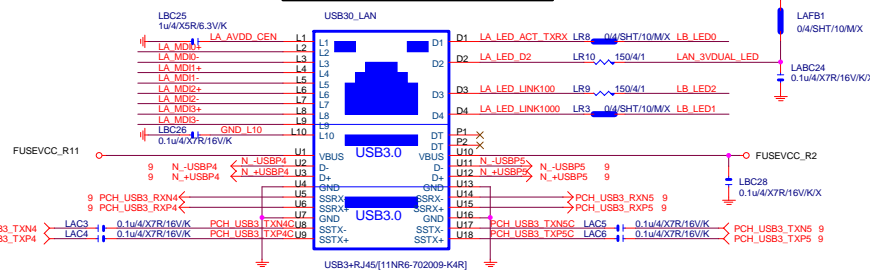
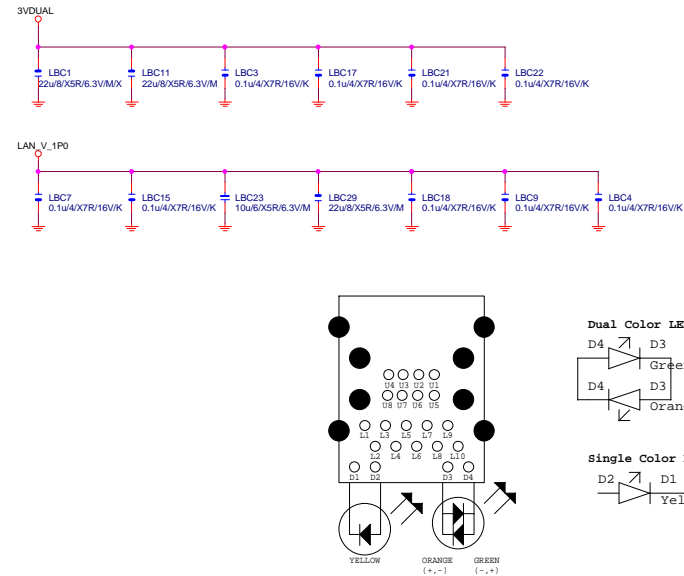
-PROCHOT:有mos heatsink不用prochot function



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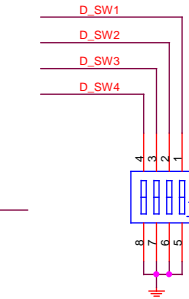
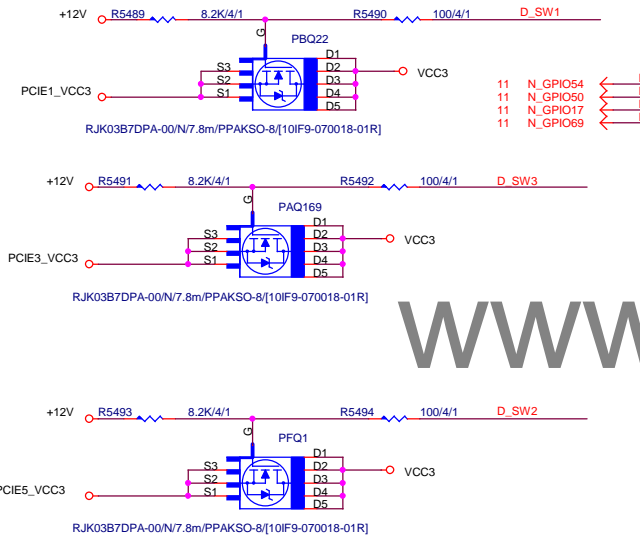
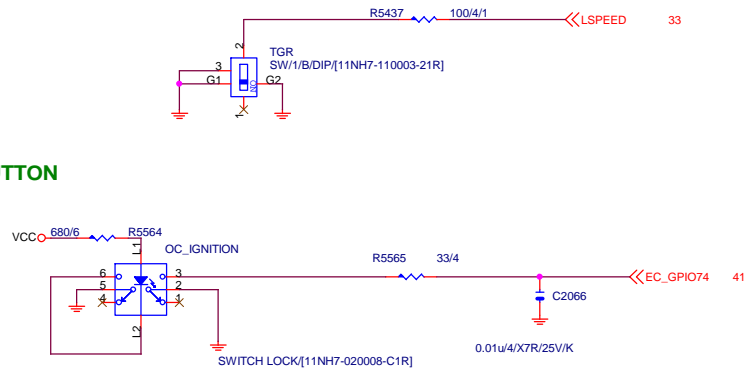
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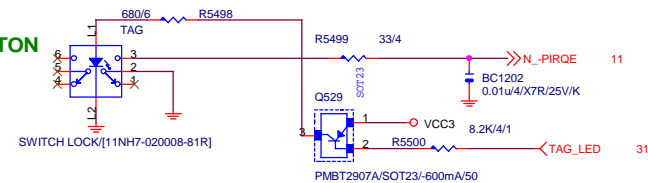
PS:視EMI需求

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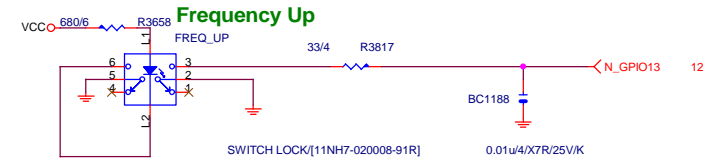
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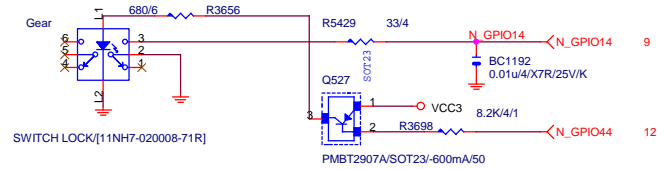
TAG BUTTON



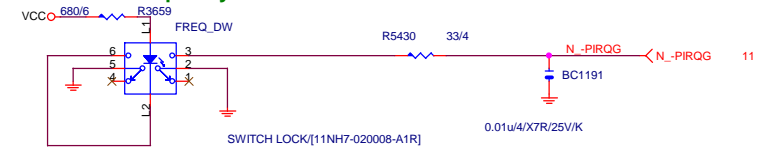
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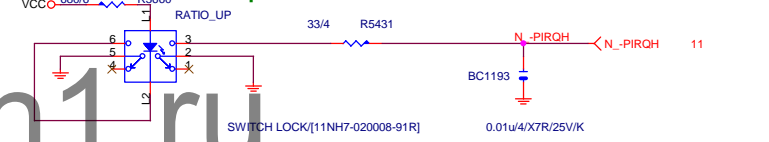
Gear



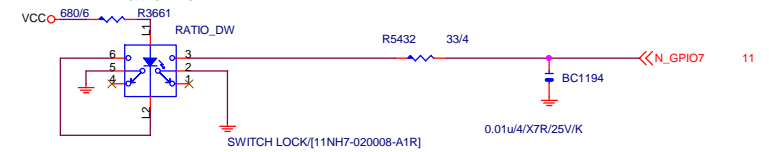
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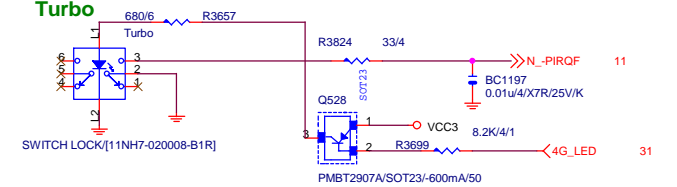
Ratio Up



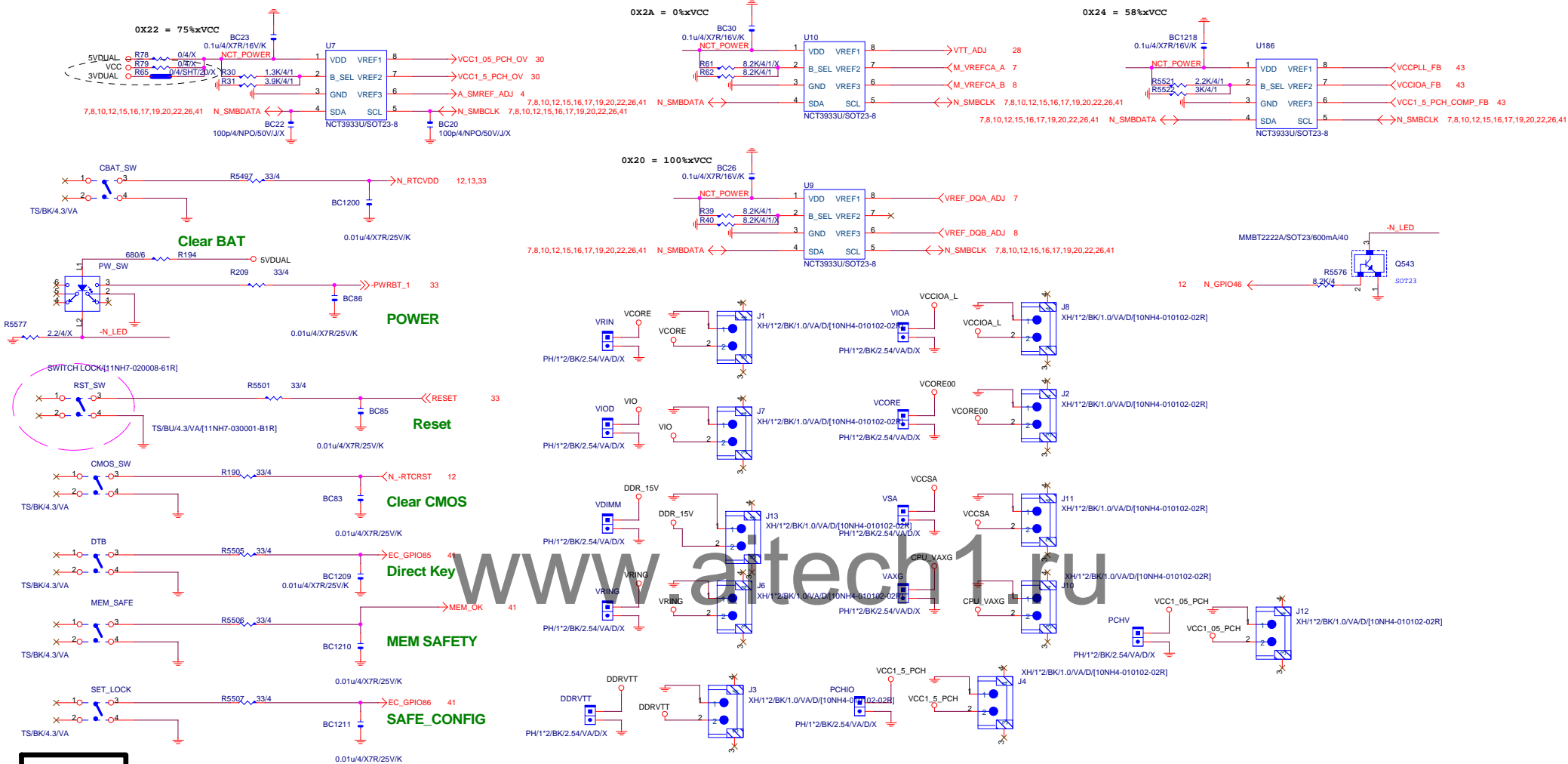
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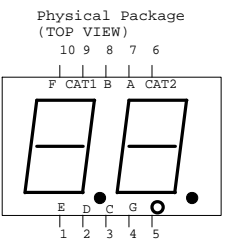
Turbo



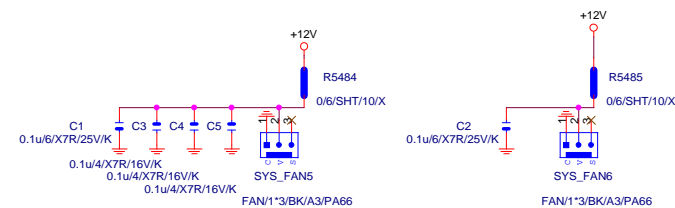
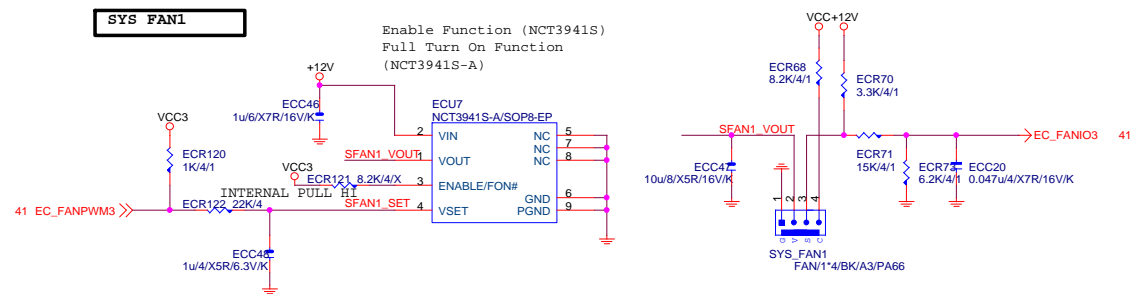
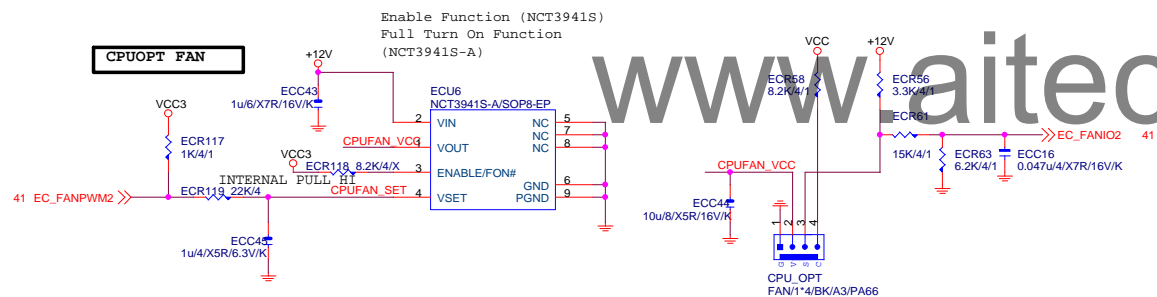
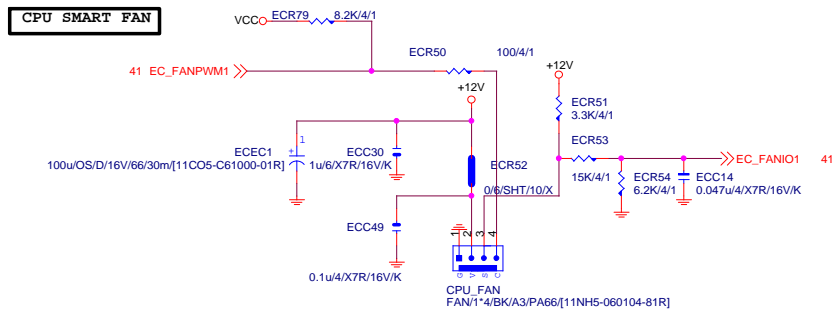
GIGABYTE™			
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SWITCH			
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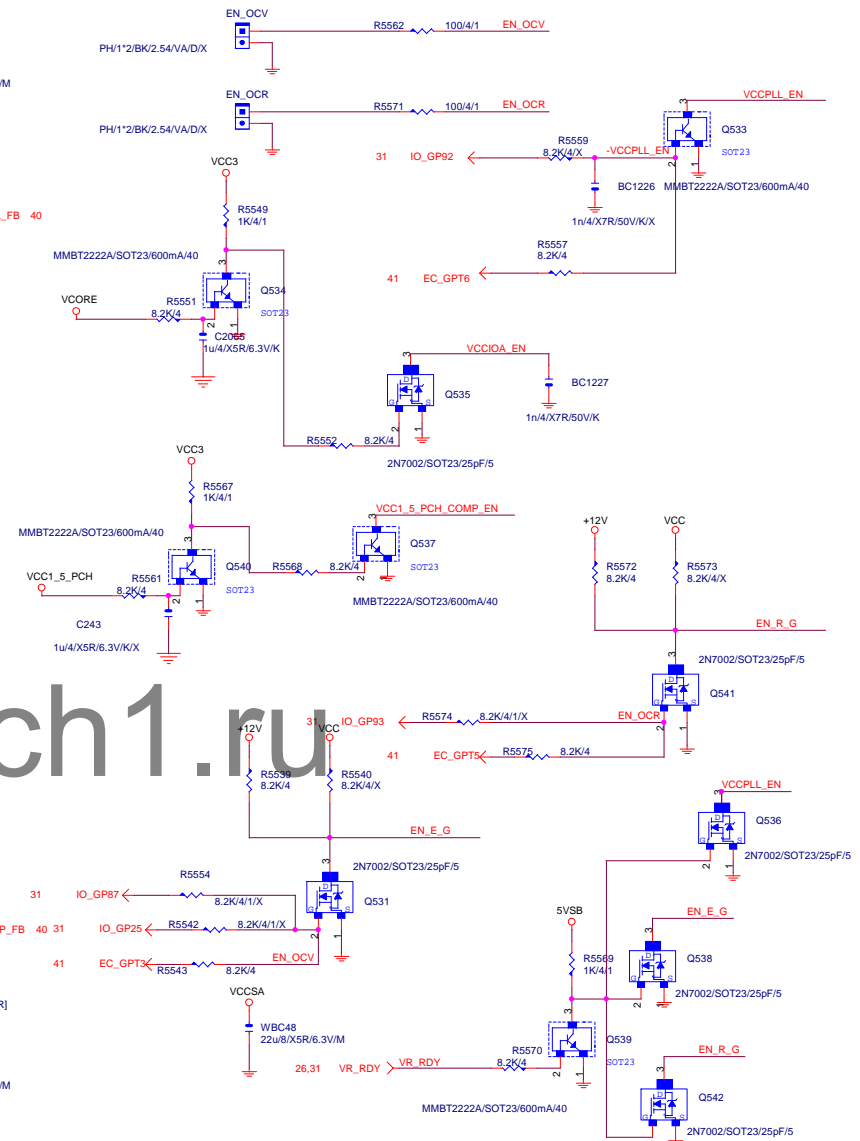
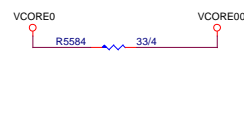
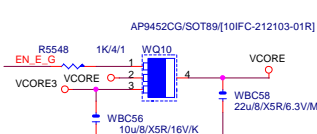
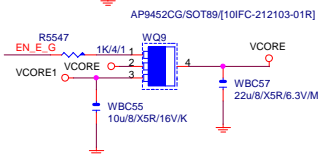
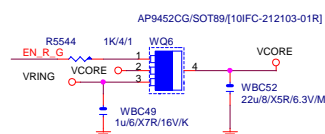
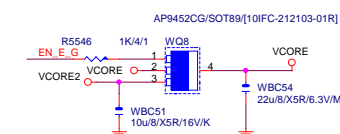
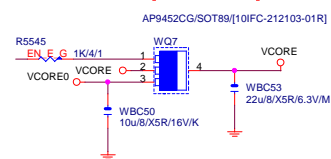
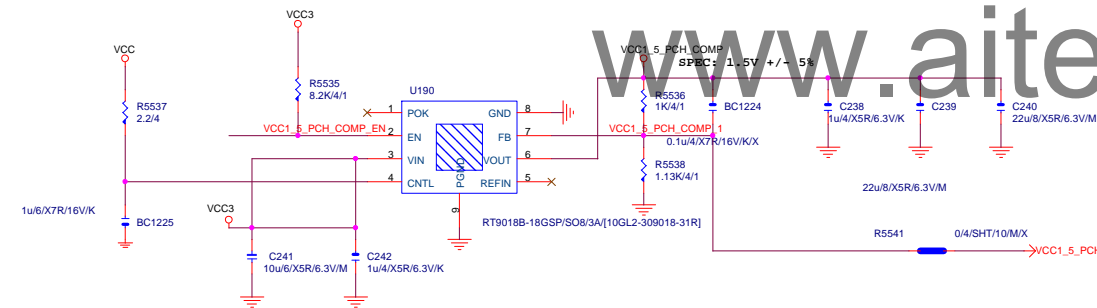
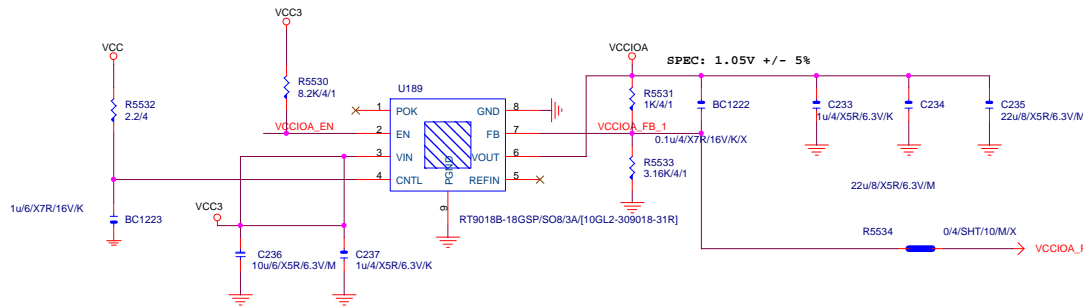
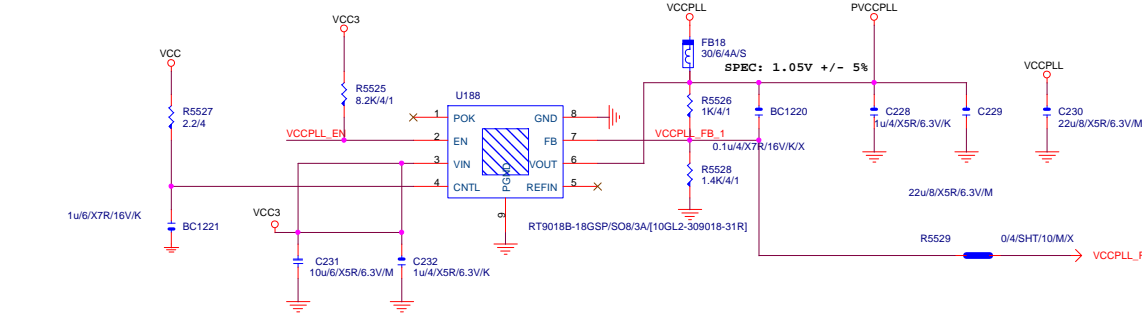


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RST, PWR, CLR_CMOS, OV			
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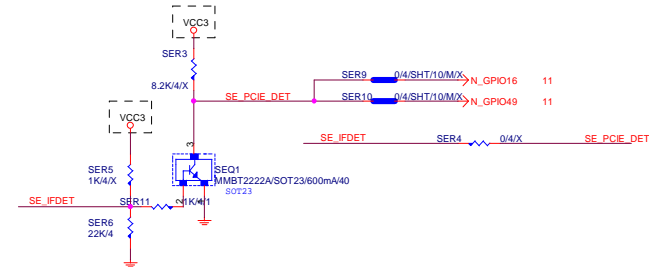
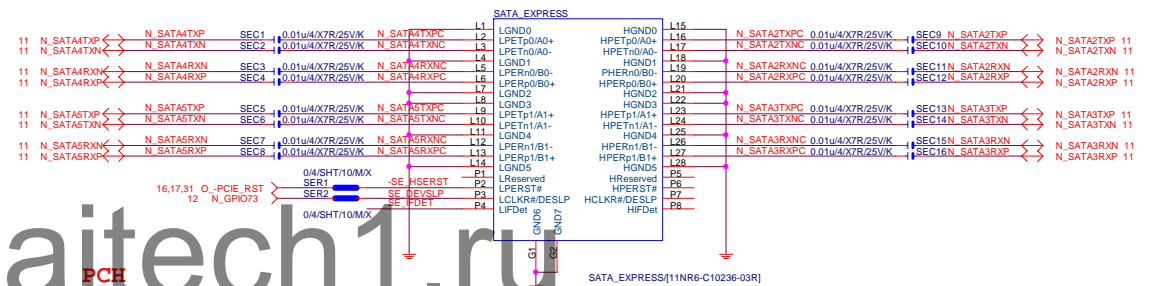
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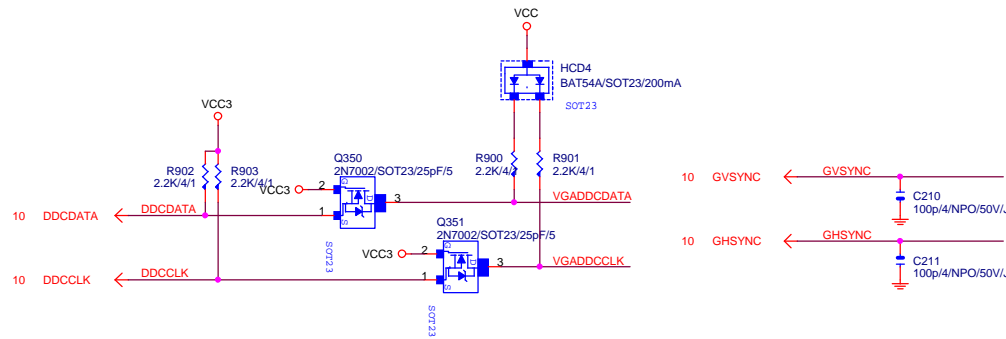
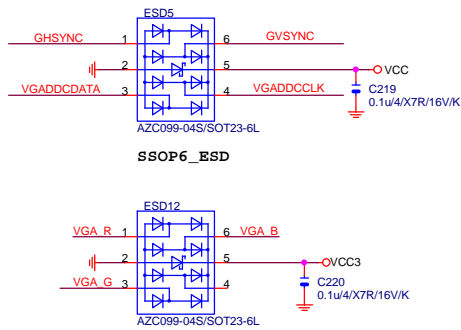
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PCH

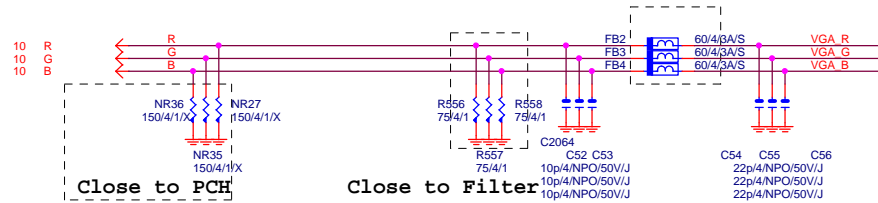


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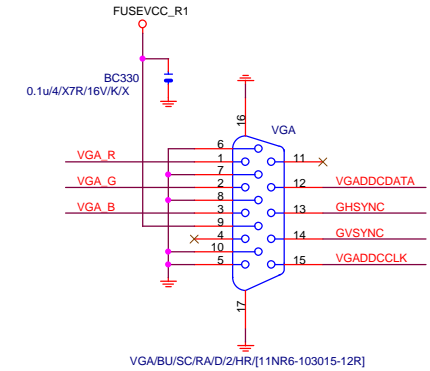
VGA ESD



VGA DDC



VGA CONNECTOR



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Title			
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Size	Document Number	1.0	Rev
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Control

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